

Plano Intel 11.6" Schematics Document

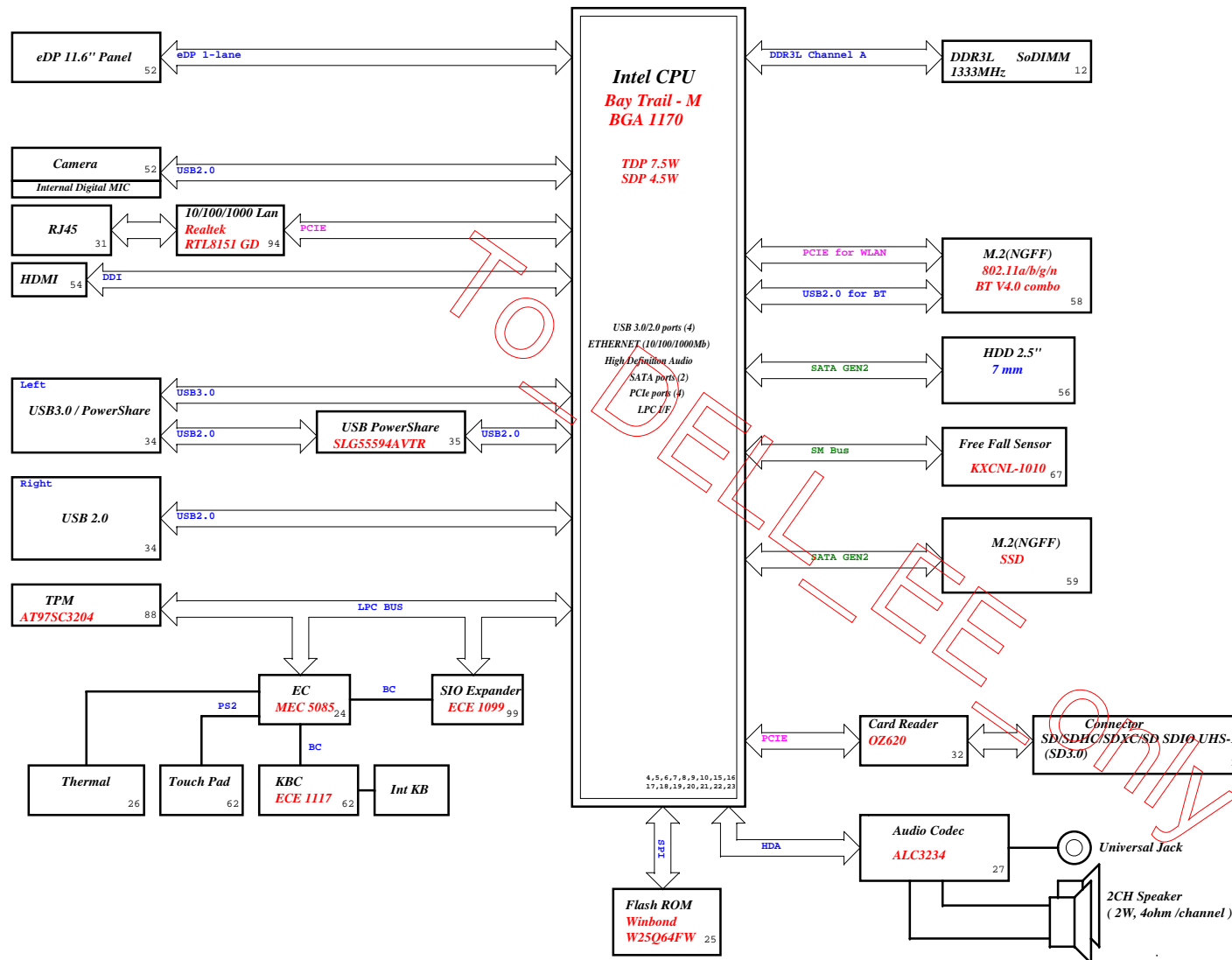
Baytrail M

2014-12-29
REV : A00

DY : None Installed
XDP: For CPU XDP Debug Port installed

Plano 11.6" Block Diagram

Project code : 4PD021010001
PCB P/N : 14230
Revision : -1



CHARGER	
BQ24715	44
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCRATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5
CPU DC/DC	
ISL95833	46-48
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE GFX_CORE
SYSTEM DC/DC	
SY8206DQNC & RT8068A	50
INPUTS	OUTPUTS
DCRATOUT	ID0V_S5 ID0V_VREF_S5
SYSTEM DC/DC	
SY8206DQNC & APL5338	49
INPUTS	OUTPUTS
DCRATOUT	ID33V_S3 ID067V_S0 ID06_VREF_S3
SYSTEM DC/DC	
S-1339D15-M5001 S-1339D18-M5T1U3	51
INPUTS	OUTPUTS
3D3V_S5	ID5V_S0 ID8V_S5
Load Switches	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0 3D3V_LAN LCDVDD
ID33V_S5 ID8V_S5 ID0V_S5	ID33V_S0 ID8V_S0 ID0V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top L2:PWR/GND L3:Signal L4:Signal L5:PWR/GND L6:Bottom	

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<Core Design>

Title			
<Title>			
Size	Document Number		Rev
A	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014	Sheet	3 of 109

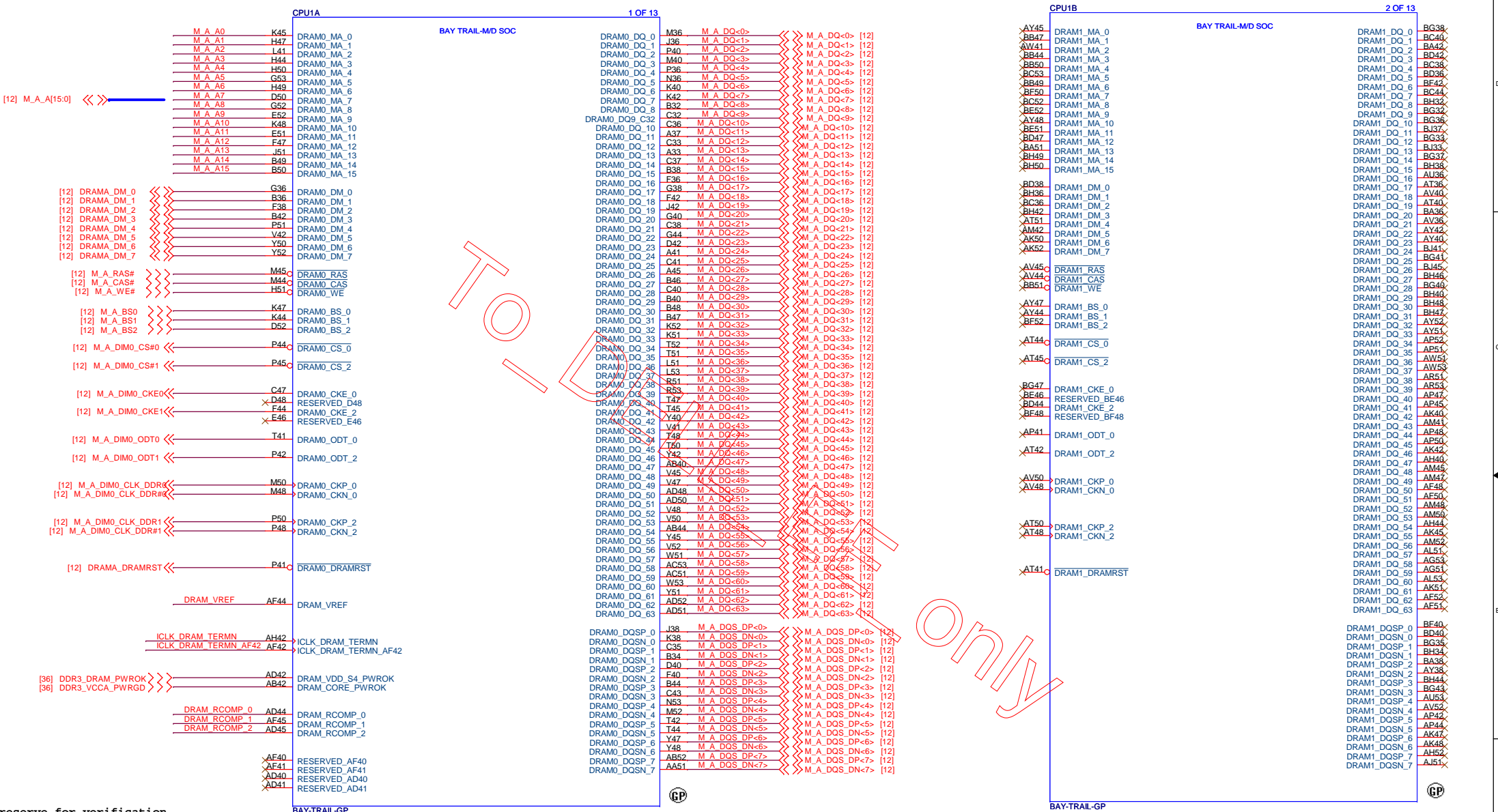
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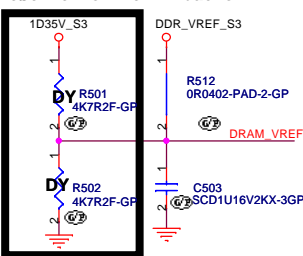
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Title			
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Size	Document Number		Rev
A	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014	Sheet	4 of 109

SSID = CPU



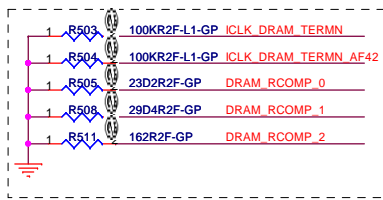
reserve for verification



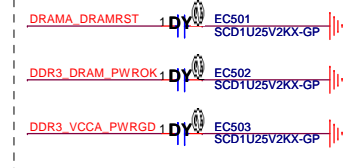
PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

NOTE: PLACE 0.1U CAP CLOSE TO CPU

Note: All RCOMP resistors have ±1% tolerance



EMI caps.



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CPU (DDR)

Plano 11.6" BTM

Date: Tuesday, December 16, 2014 Sheet 5 of 109


SSID = CPU

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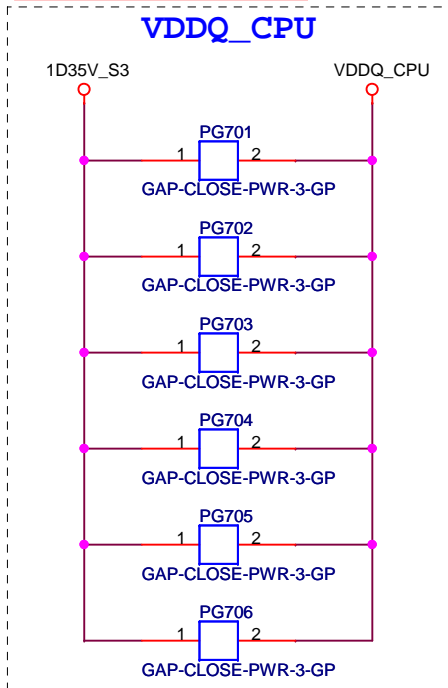
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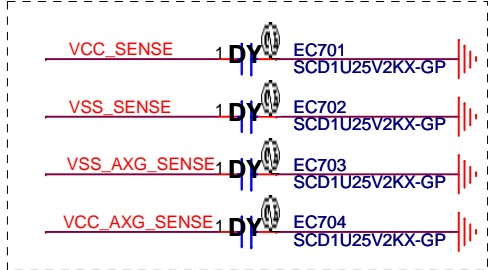
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Title CPU (CFG)		
Size A4	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014	Sheet 6 of	109

SSID = CPU



EMI Caps.



Parallel

[47] VCC_SENSE <<<
[47] VSS_SENSE <<<

Parallel

[48] VSS_AXG_SENSE <<<
[48] VCC_AXG_SENSE <<<

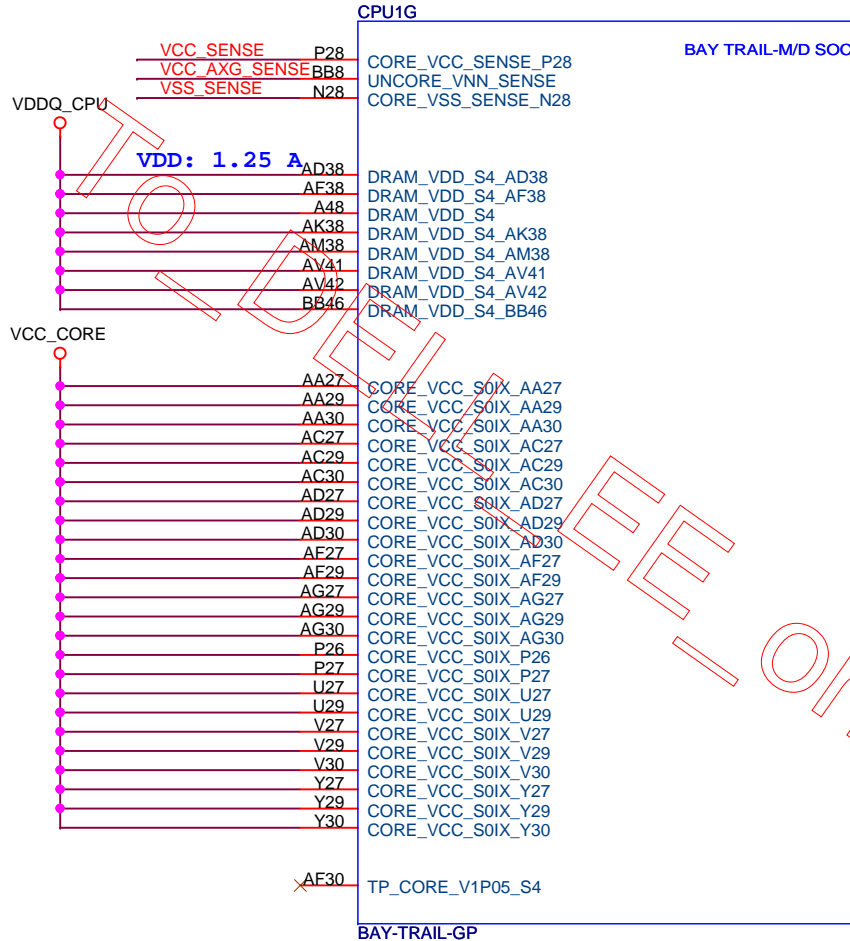
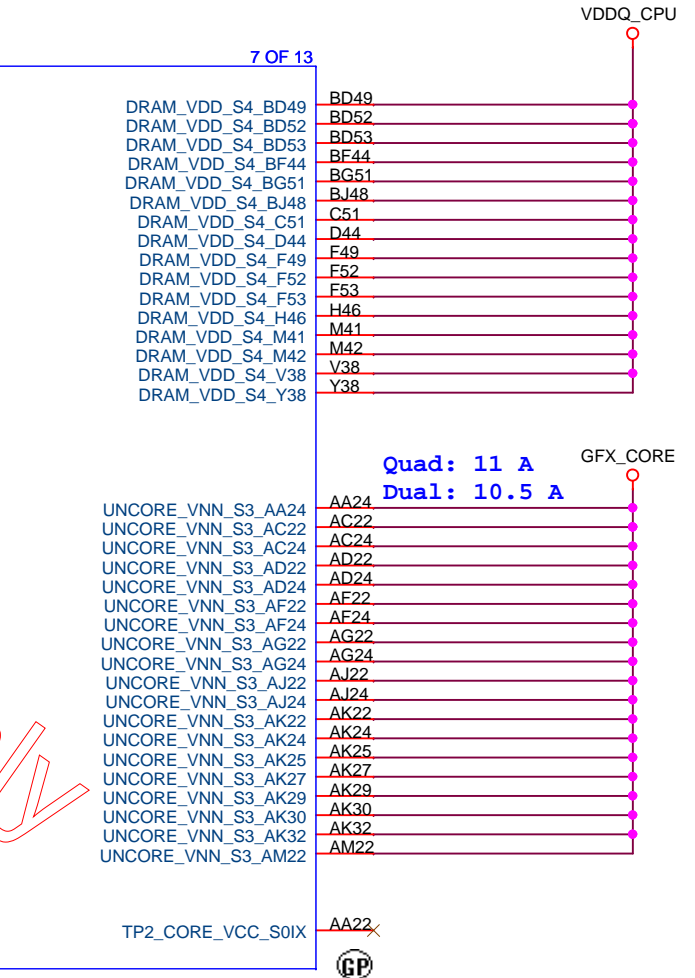


Table 53. VCC and VNN Currents

SKU	VCC Icc Max	VNN Icc Max
N3520 - Quad Core Pentium	10.5 A	10.5 A
N2920 - Quad Core Celeron	8.5 A	10.5 A
N2820 - Dual Core Celeron	5.2 A	10.5 A
N2815 - Dual Core Celeron	5.2 A	10.5 A
N2806 - Dual Core	4 A	7 A
J2900 - Quad Core Pentium	13.5 A	11 A
J1900 - Quad Core Celeron	10.5 A	11 A
J1800 - Dual Core Celeron	7 A	10.5 A



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Title

CPU (VCC CORE)

Size
A4

Document Number

Plano 11.6" BTM

Rev

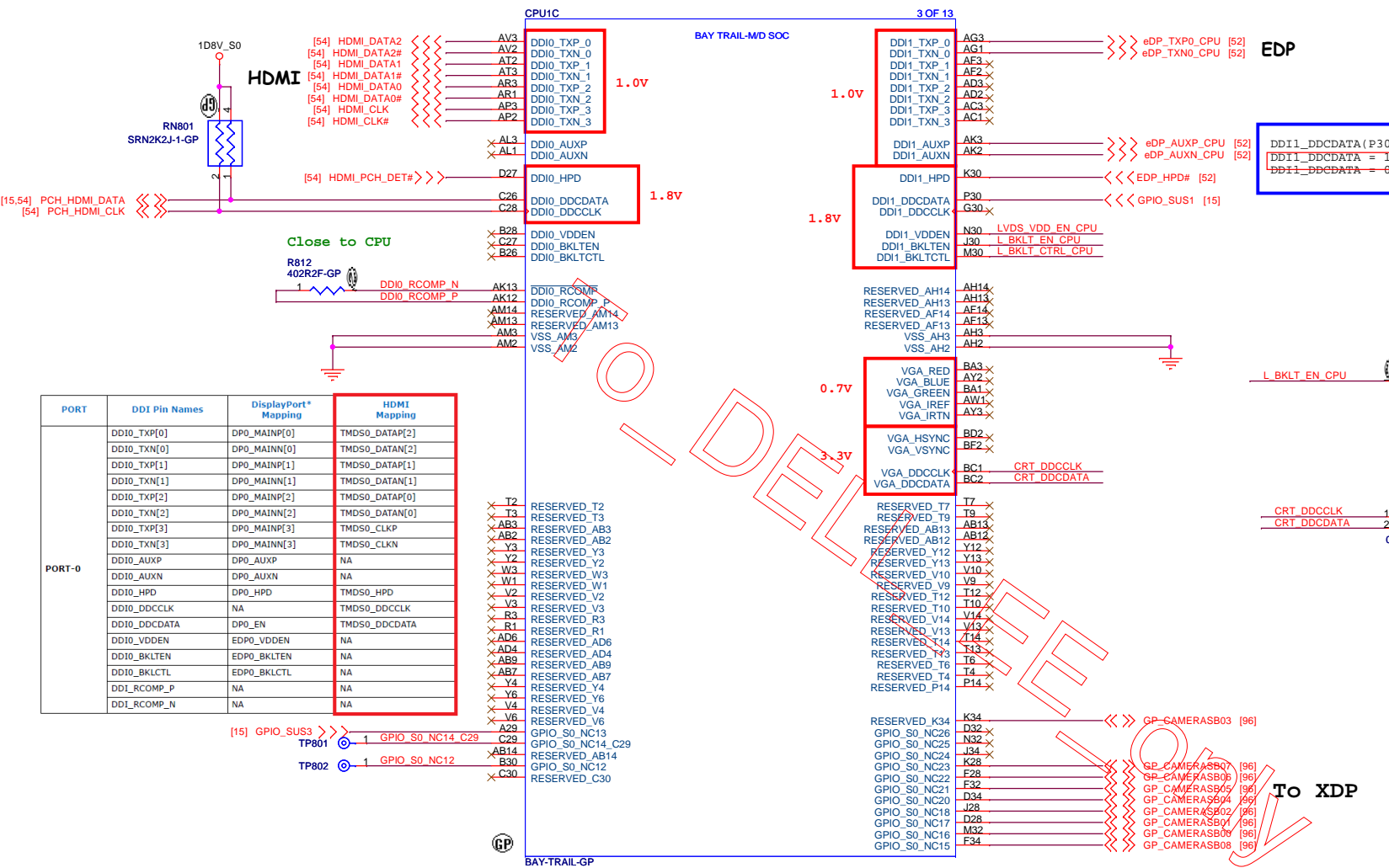
A00

Date: Tuesday, December 16, 2014

Sheet 7 of 109

SSID = CPU

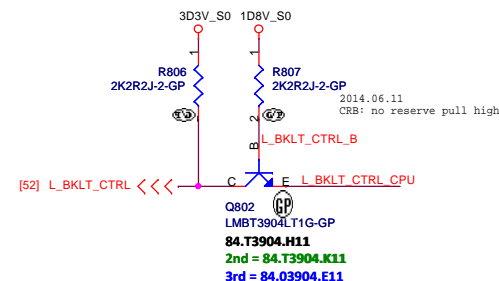
DDI0_DDCDATA(C26): Strap Pin for DDI0 Detect
DDI0_DDCDATA = 1 DDI0 detected
DDI0_DDCDATA = 0 DDI0 not detected



EDP

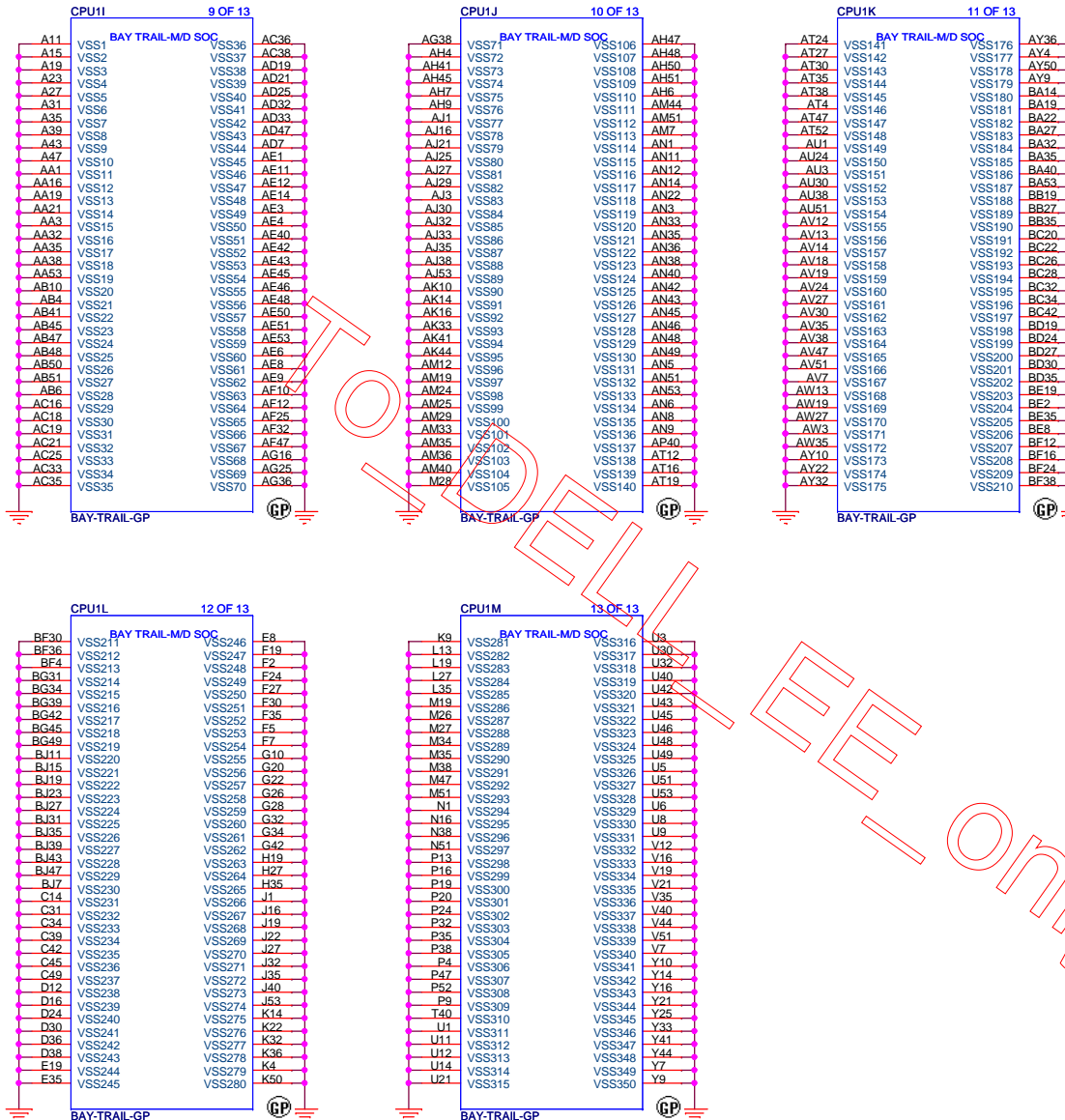
DDI1_DDCDATA(P30): Strap Pin for DDI1 Detect
DDI1_DDCDATA = 1 DDI1 detected
DDI1_DDCDATA = 0 DDI1 not detected

Level shift



<Core Design>

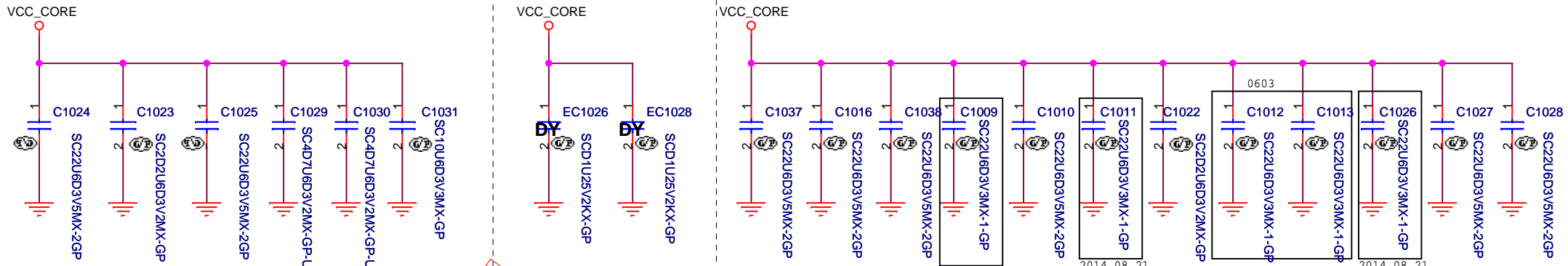
SSID = CPU



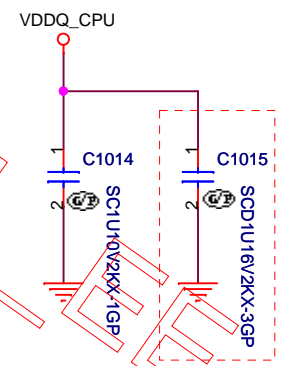
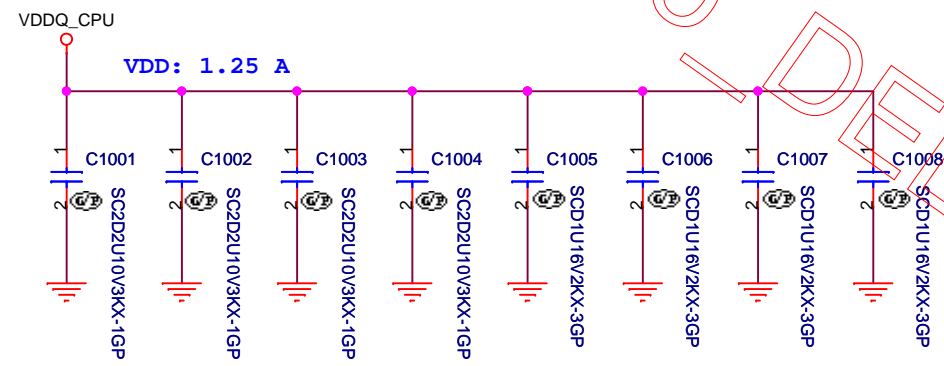
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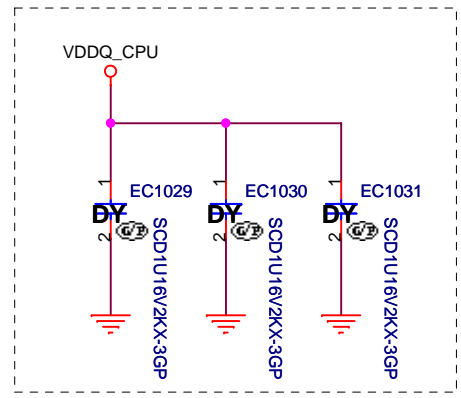
DELL		Wistron Corporation	
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Title			
CPU (VSS)			
Size	Document Number	Rev	
A3	Plano 11.6" BTM	A00	
Date:	Tuesday, December 16, 2014	Sheet	9 of 109



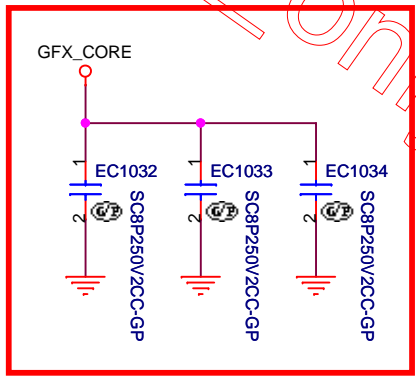
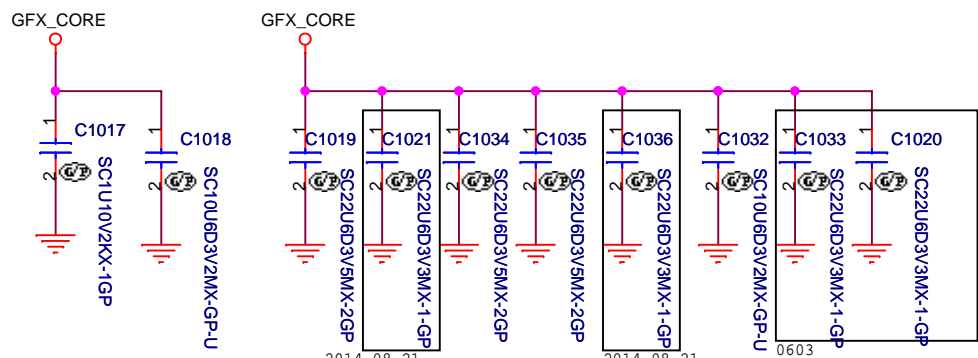
EMI Caps.



close to pin AD38 & AF38



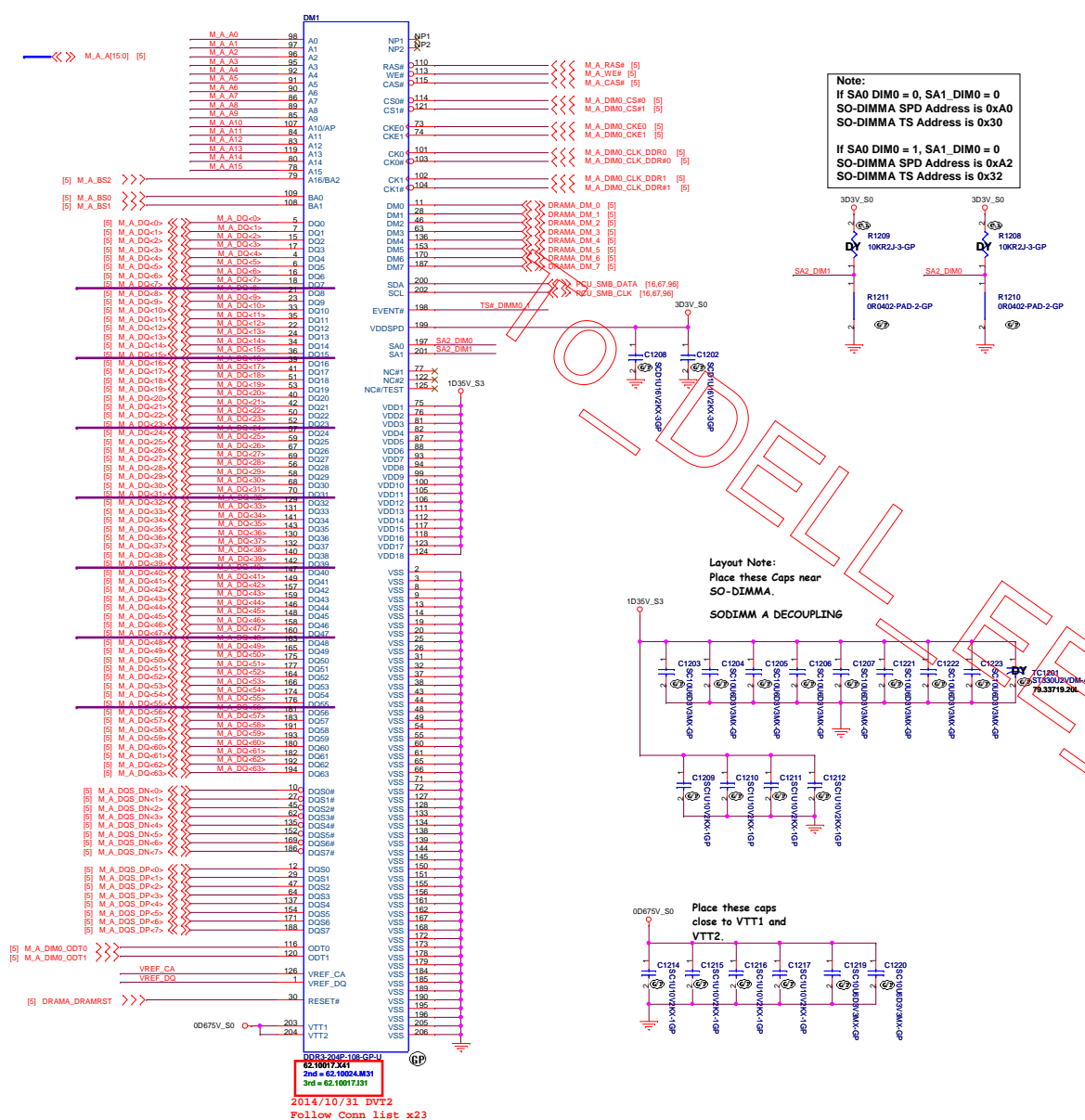
EMI Caps.



10/24/2014 DVT2 modify RF Caps.

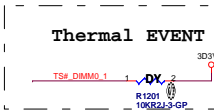
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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 10 of 109	

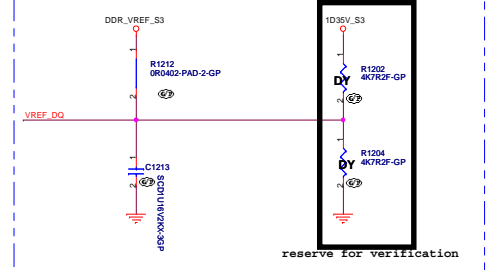


Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

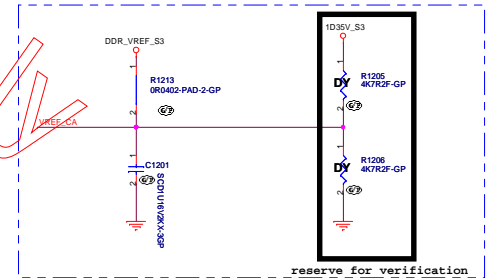
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



For Intel Recommend Close to DIMM(Bay trail M)

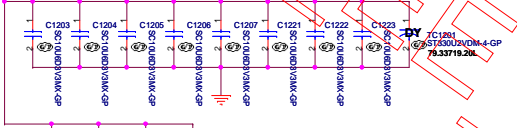


For Intel Recommend Close to DIMM(Bay trail M)

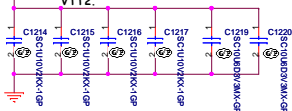


Layout Note:
Place these Caps near
SO-DIMMA.

SODIMM A DECOUPLING



Place these caps
close to VTT1 and
VTT2.




DDR3-1600-108-GP-1
2nd = 62.10017.341
3rd = 62.10017.331
2014/10/31 DVT2
Follow Conn list x23

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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014	Sheet	13	of 109

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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014	Sheet	14	of 109

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap (A16 Override)
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [056]
Schematic						
High	SPI (Default) <small>Internal PH</small>	Normal Operation (Default) <small>Internal PH</small>	DDI0 detected	DDI1 detected	DDI1 detected	Top address bit is unchanged (Default) <small>Internal PH</small>
Low	LPC	Override	DDI0 not detected (Default)	DDI1 not detected (Default)	DDI1 not detected	Top address bit is inverted

Removed MDSI strap pin.

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

Signal Name	Dir	Term	Plat. Power
GPIO_S0_SC[056]†	I/O	20k,H	V1P8S
GPIO_S0_SC[063]†	I/O	20k,H	V1P8S
GPIO_S0_SC[065]†	I/O	20k,H	V1P8S

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

Signal Name	Dir	Term	Plat. Power
DDI0_DDCDATA†	I/O	20k(L)	V1P8S
DDI1_DDCDATA†	I/O	20k(L)	V1P8S

INTEL BTM EDS Rev2.5

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Title			CPU(STRAP)	
Size A3	Document Number	Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014	Sheet 15	of 109		

SSID = PCH

Close to CPU

Avoid routing next to clock/high speed signals.

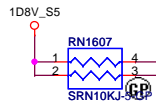
Connected to package ground.

USB 3.0(power share)

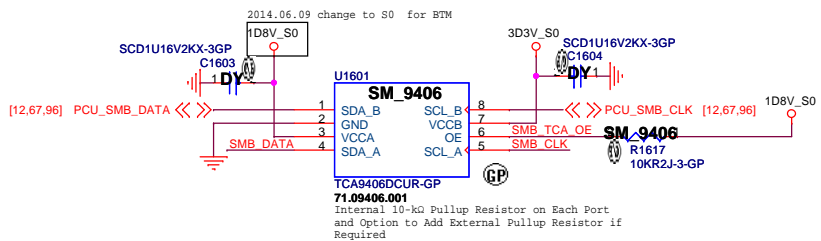
USB 2.0

WLAN

Camera



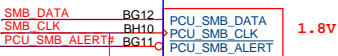
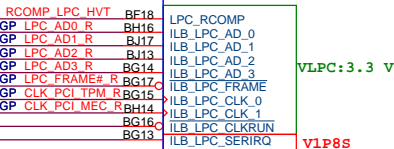
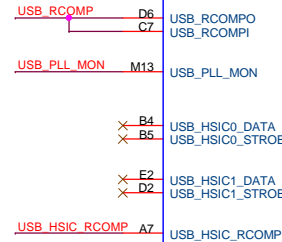
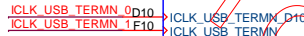
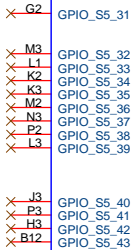
PCU_SMB_ALERT#	I (OD) TBD	SMBus Alert
		This signal is used by SMBus devices to wake the system or generate SM#*. This signal is open drain, and it has 20 kΩ internal pull-up. This signal is muxed and may be used as a GPIO.



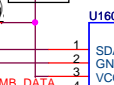
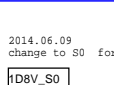
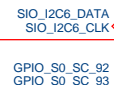
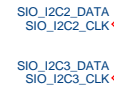
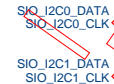
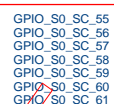
CPU1F

BAY TRAIL-MD SOC

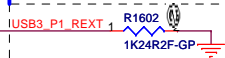
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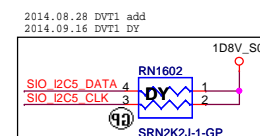
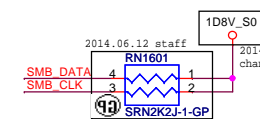
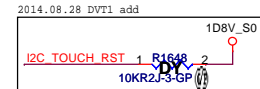
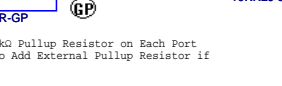
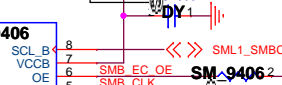
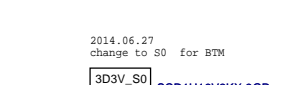
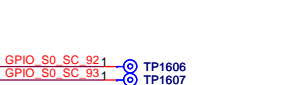
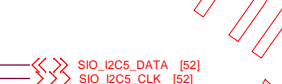
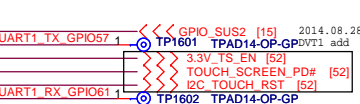
BAY-TRAIL-GP



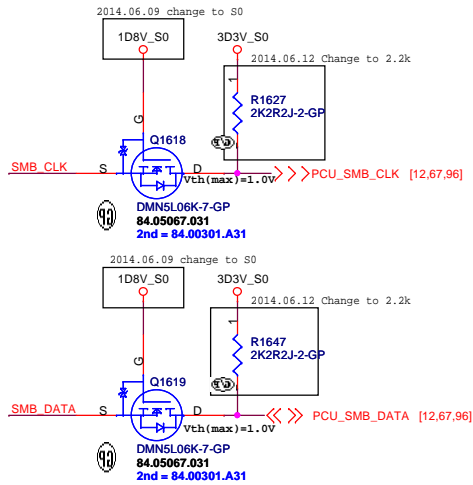
Make sure the signal routing is as short as possible and isolated from high speed data signal. Parasitic resistance for the overall routing should be less than 100 Ω.



GPIO_S0_SC [56](BC12): Top swap (A16 Override)
GPIO_S0_SC_56 = 1 Top address bit is unchanged (Default)
GPIO_S0_SC_56 = 0 Top address bit is inverted



Level shift



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CPU (USB/LPC/GPIO)

Size A3 Document Number **Plano 11.6" BTM** Rev **A00**

Date: Friday, December 19, 2014 Sheet 16 of 109

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Title

CPU (Reserved)

Size
A4

Document Number

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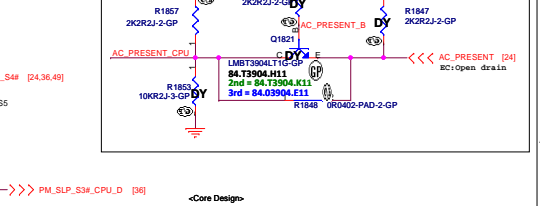
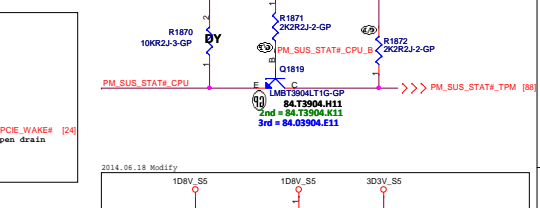
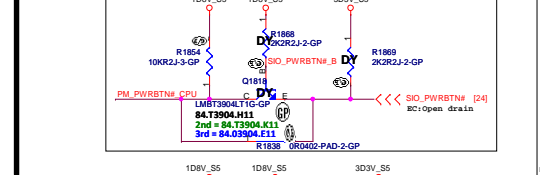
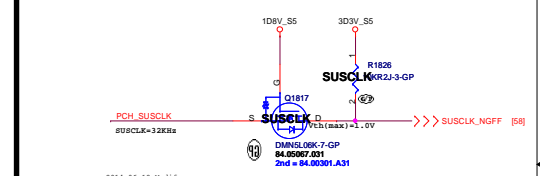
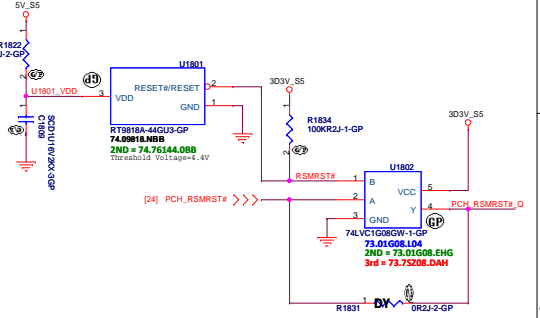
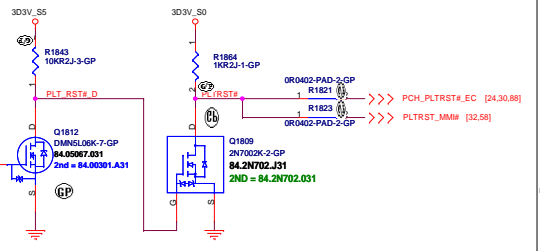
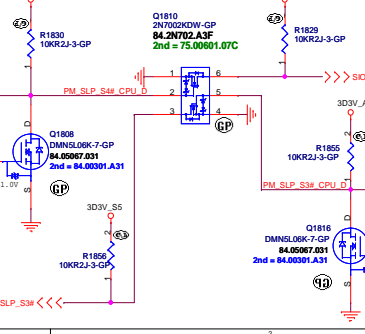
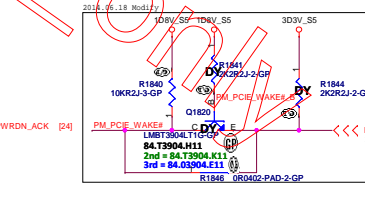
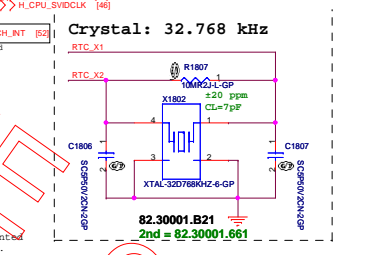
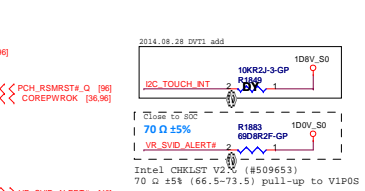
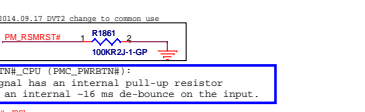
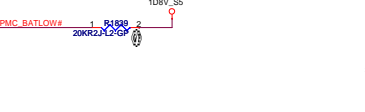
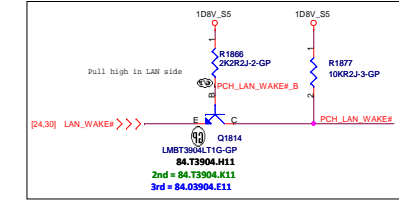
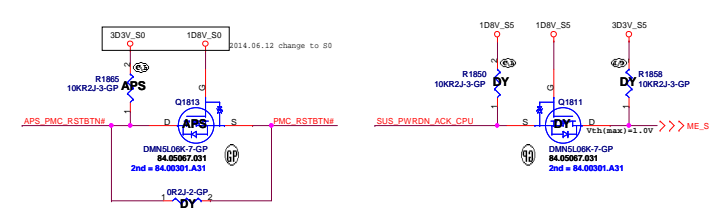
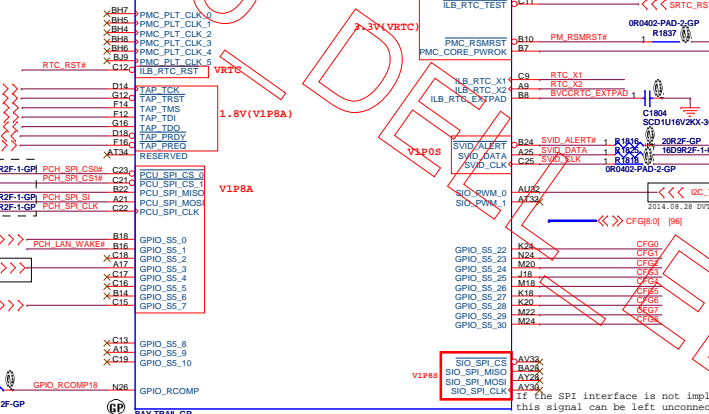
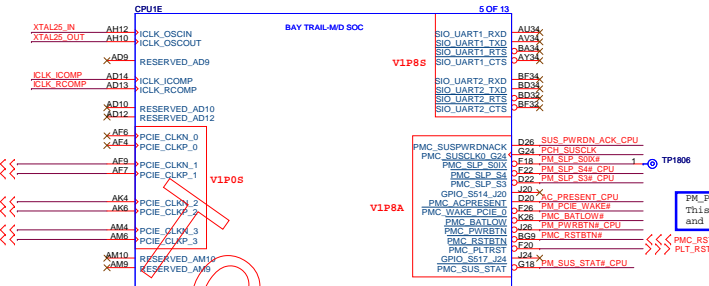
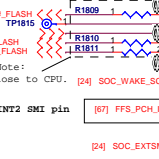
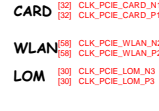
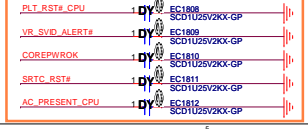
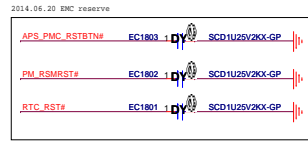
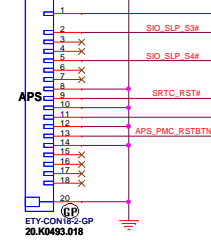
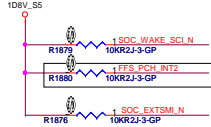
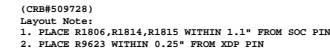
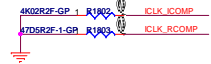
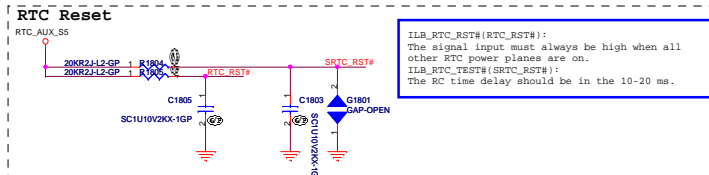
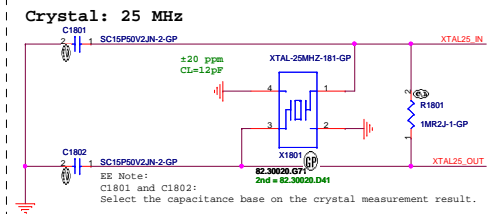
Rev

A00

Date: Monday, December 22, 2014

Sheet 17 of 109

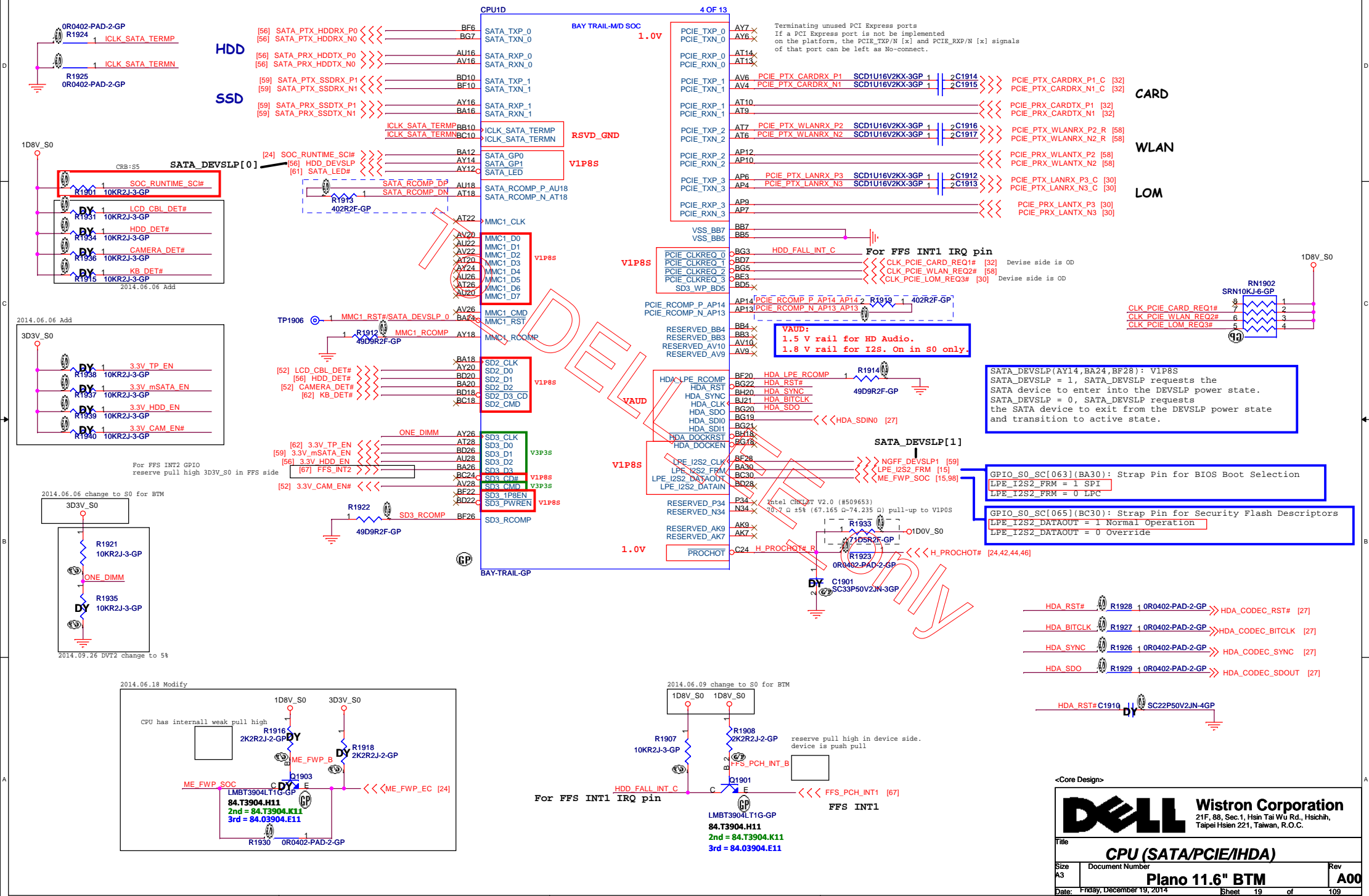
SSID = PCH



SSID = PCH

SATA_GP:
When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.

Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.




SSID = PCH

Blanking

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Title

Reserved

Size A4	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014	Sheet 20 of	109

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A4

Document Number

Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014


Sheet 22 of 109

SSID = PCH

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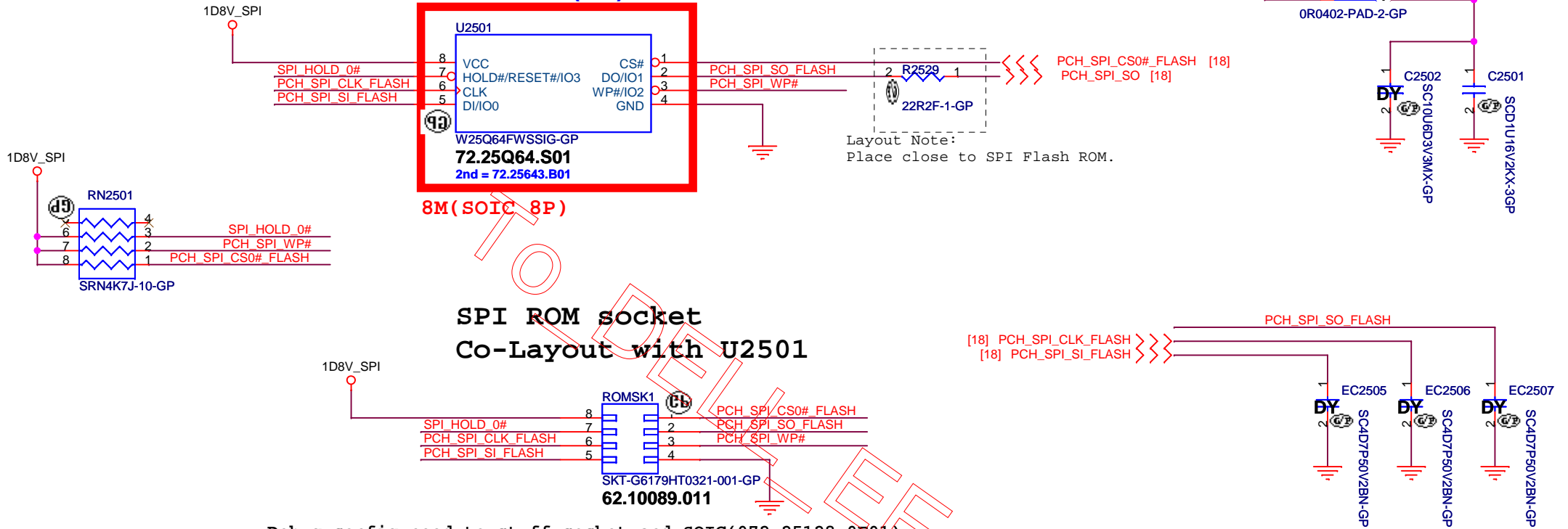
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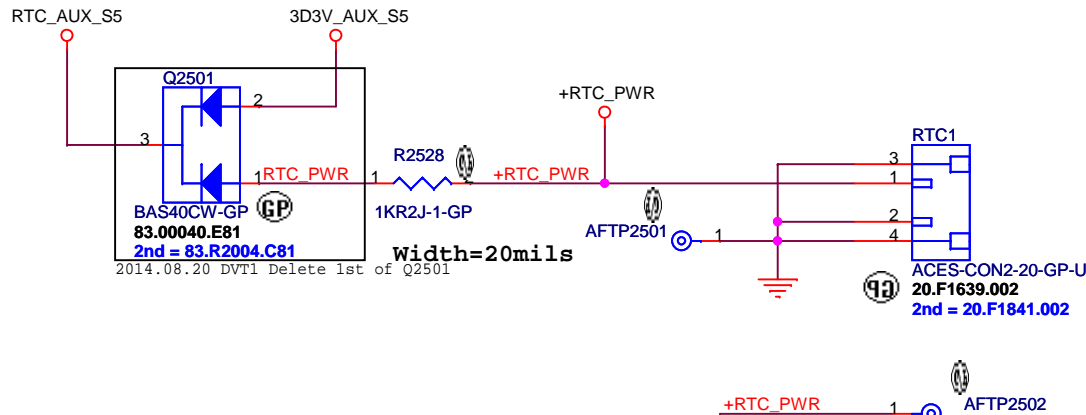
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Title CPU (VSS)			
Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014	Sheet	23	of 109

SSID = Flash.ROM

SYSTEM SPI ROM SPI Flash ROM(8M) for PCH



SSID = RTC



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Title

Flash/RTC

Size
A4

Document Number

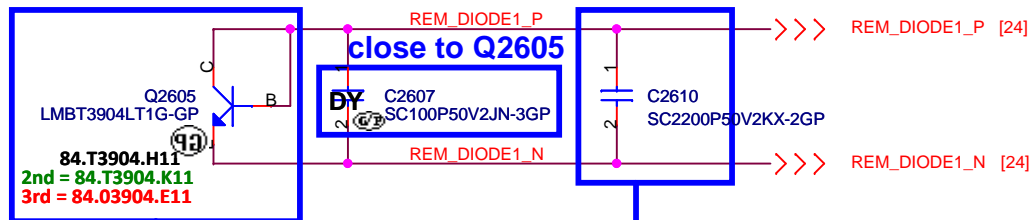
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

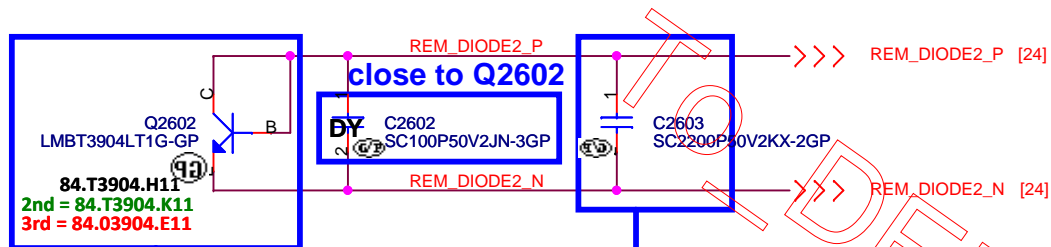
Sheet 25 of 109

SSID = Thermal

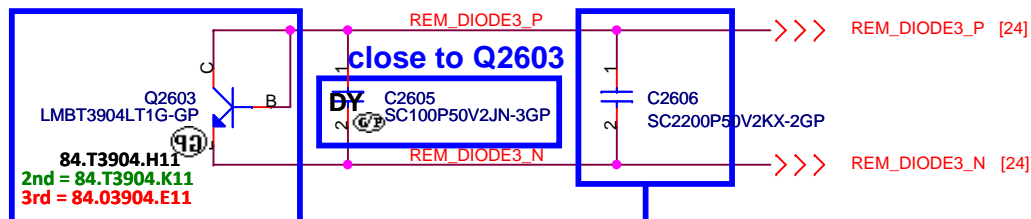


Channel 1 is for CPU
Channel 2 is for DIMM
Channel 3 is for KB Skin
Channel 4 is for WLAN

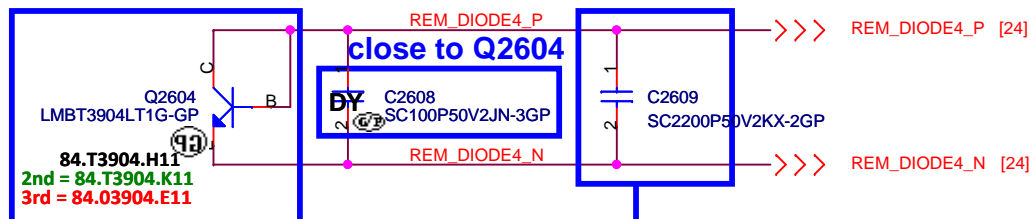
Layout Note: close to MEC5085 within 400 mil
Layout Note: Place to OTP, C2607 could close to Q2605
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



Layout Note: close to MEC5085 within 400 mil
Layout Note: Place to DIMM
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



Layout Note: close to MEC5085 within 400 mil
Layout Note: Place to KB
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



Layout Note: close to MEC5085 within 400 mil
Layout Note: Place to WLAN
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

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Title

Thermal

Size
A4

Document Number

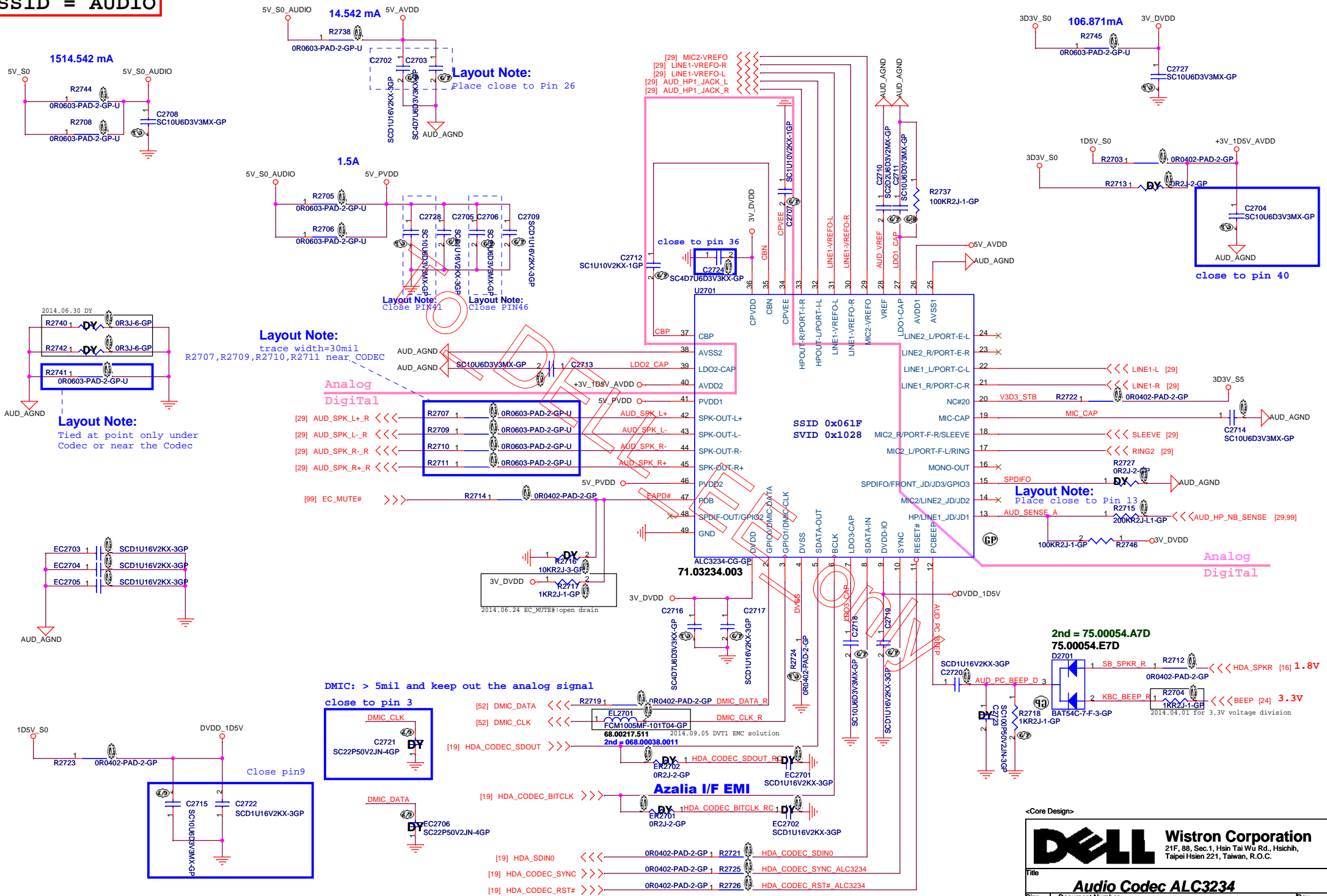
Plano 11.6" BTM

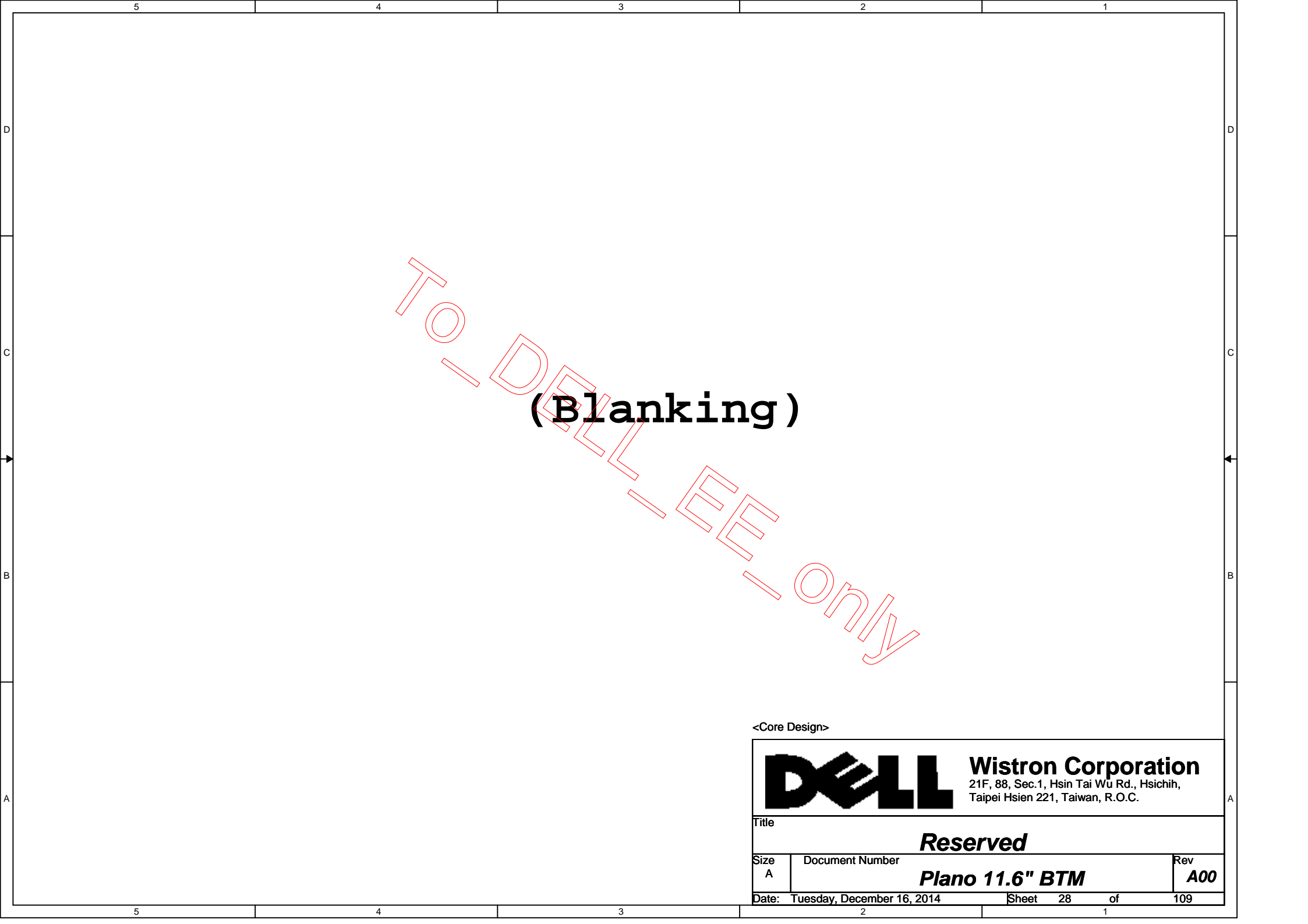
Rev
A00

Date: Tuesday, December 16, 2014

Sheet 26 of 109

SSID = AUDIO





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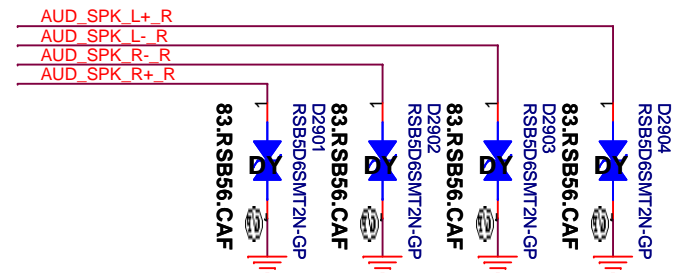
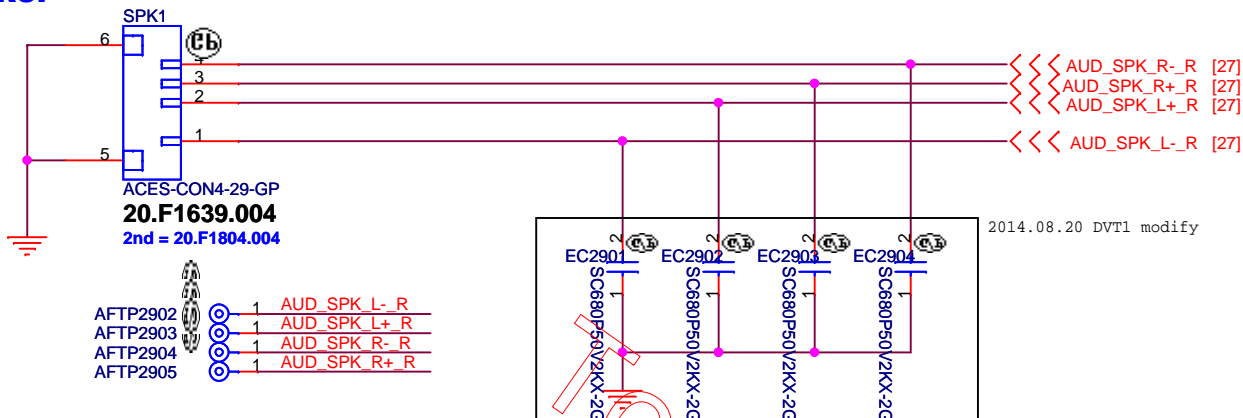
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 28 of	109

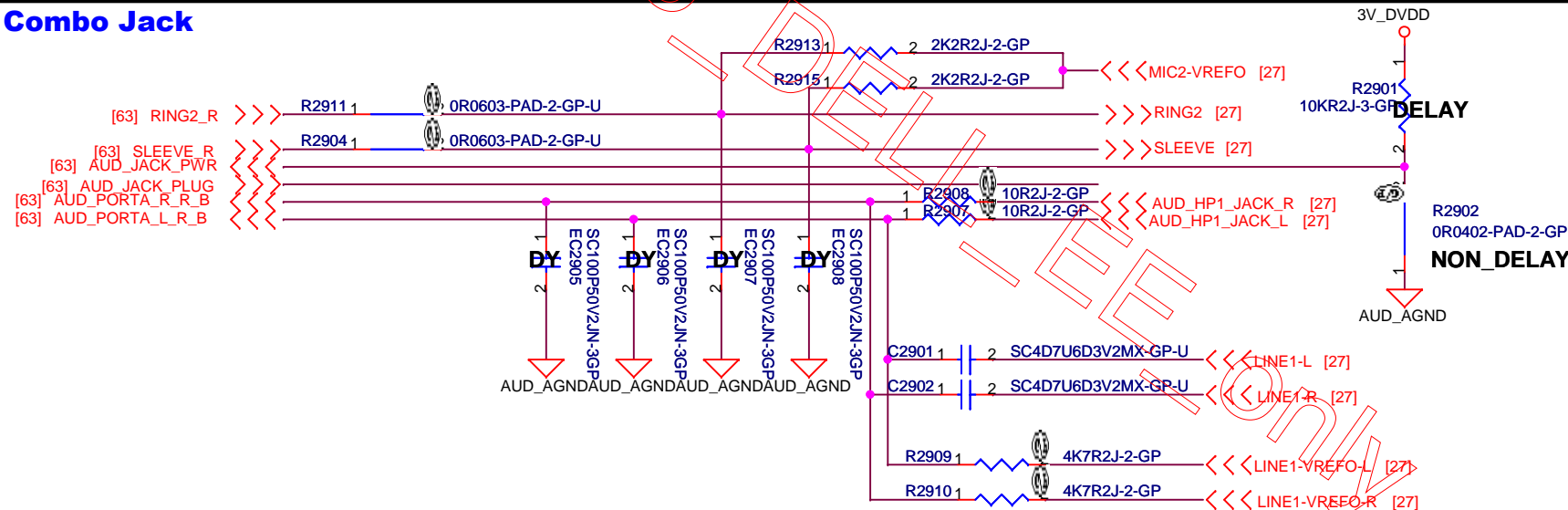
SSID = AUDIO

Speaker

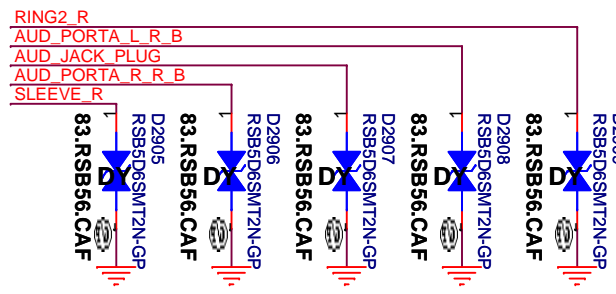
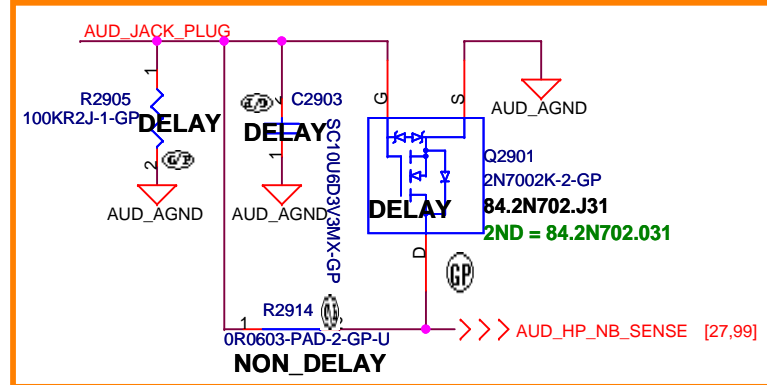
2W/ch



Combo Jack



Delay circuit



<Core Design>

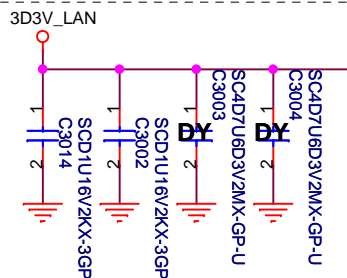


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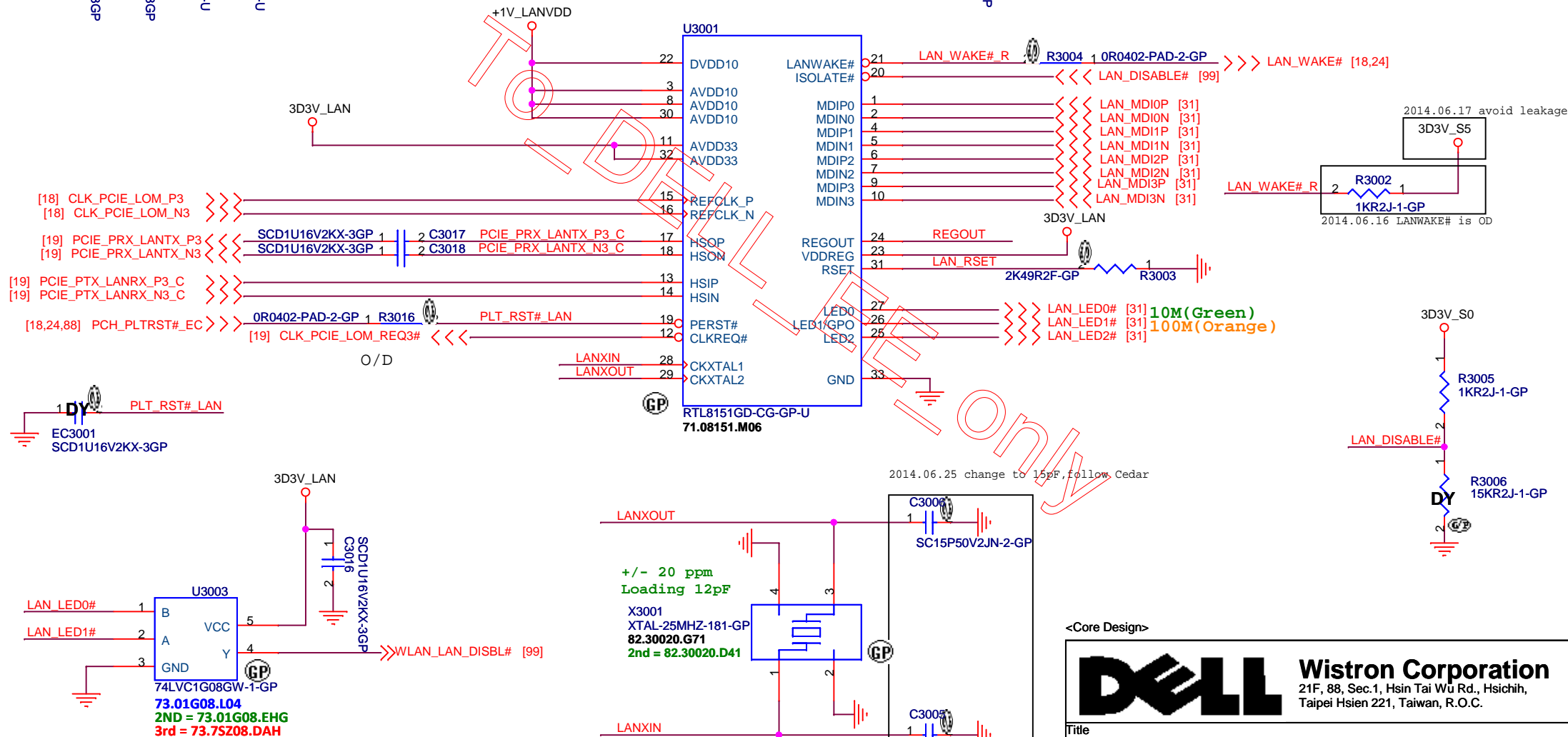
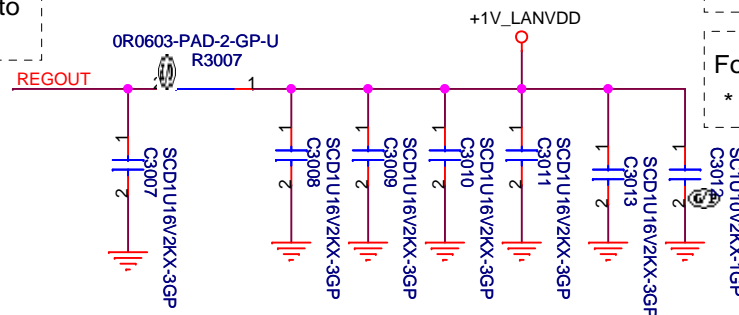
Title		
Speaker/HPMIC CONN		
Size	Document Number	Rev
A4	Plano 11.6" BTM	A00
Date:	Friday, December 19, 2014	Sheet 29 of 109

* Place C3001 and C3002 close to each AVDD33 pin-- 11, 32
* For surge improvement, place C3003 and C3004 close to each AVDD33 pin-- 11, 32. (optional)



* Place C3008 ~ C3011 close to each VDD10 pin-- 3, 8, 22, 30

* Place C3012 and C3013 close to each VDD10 pin-- 22



2014.06.25 change to 15pF, follow Cedar

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Title

LOM RTK8111G

Size

Document Number

Plano 11.6" BTM

Date: Tuesday, December 16, 2014

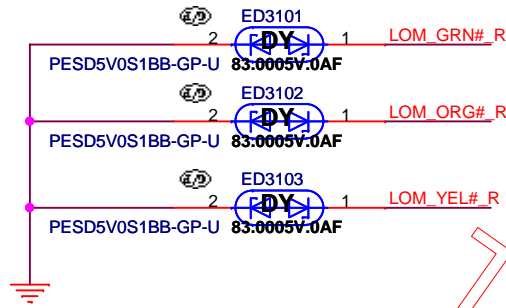
Sheet 30 of 31

Rev

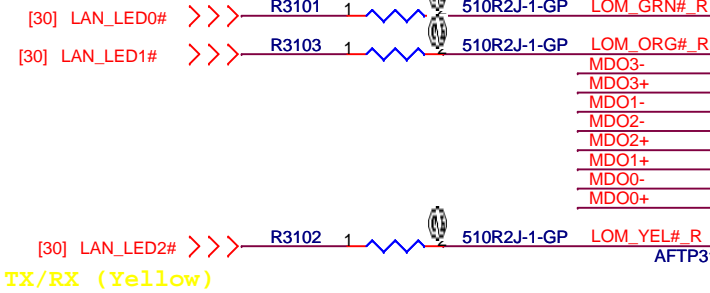
A00

109

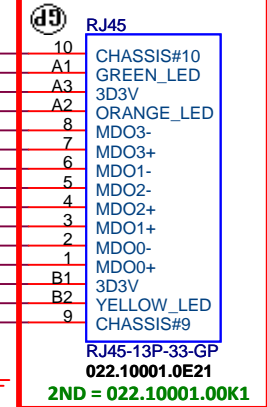
SSID = LOM



10M(Green)
100M(Orange)
1000M(Green+Orange)

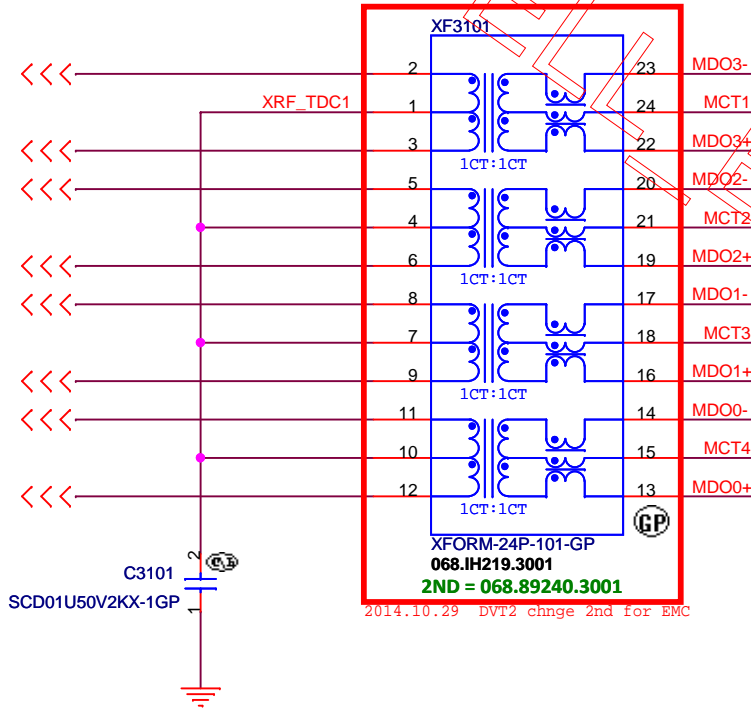


LAN TX/RX (Yellow)

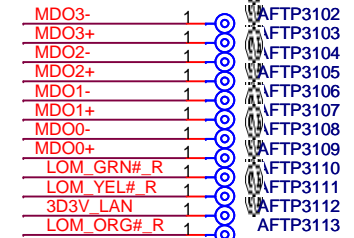
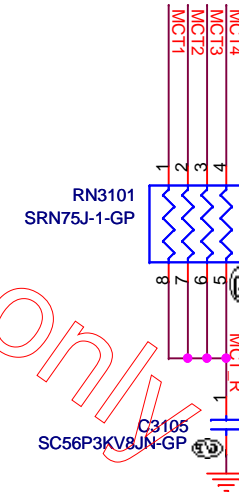


2014.10.31 DVT2
add 2nd, follow Conn list X23

[30] LAN_MDI3N
[30] LAN_MDI3P
[30] LAN_MDI2N
[30] LAN_MDI2P
[30] LAN_MDI1N
[30] LAN_MDI1P
[30] LAN_MDI0N
[30] LAN_MDI0P



2014.10.29 DVT2 change 2nd for EMC



<Core Design>



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Title

RJ45/Transformer

Size
A4

Document Number

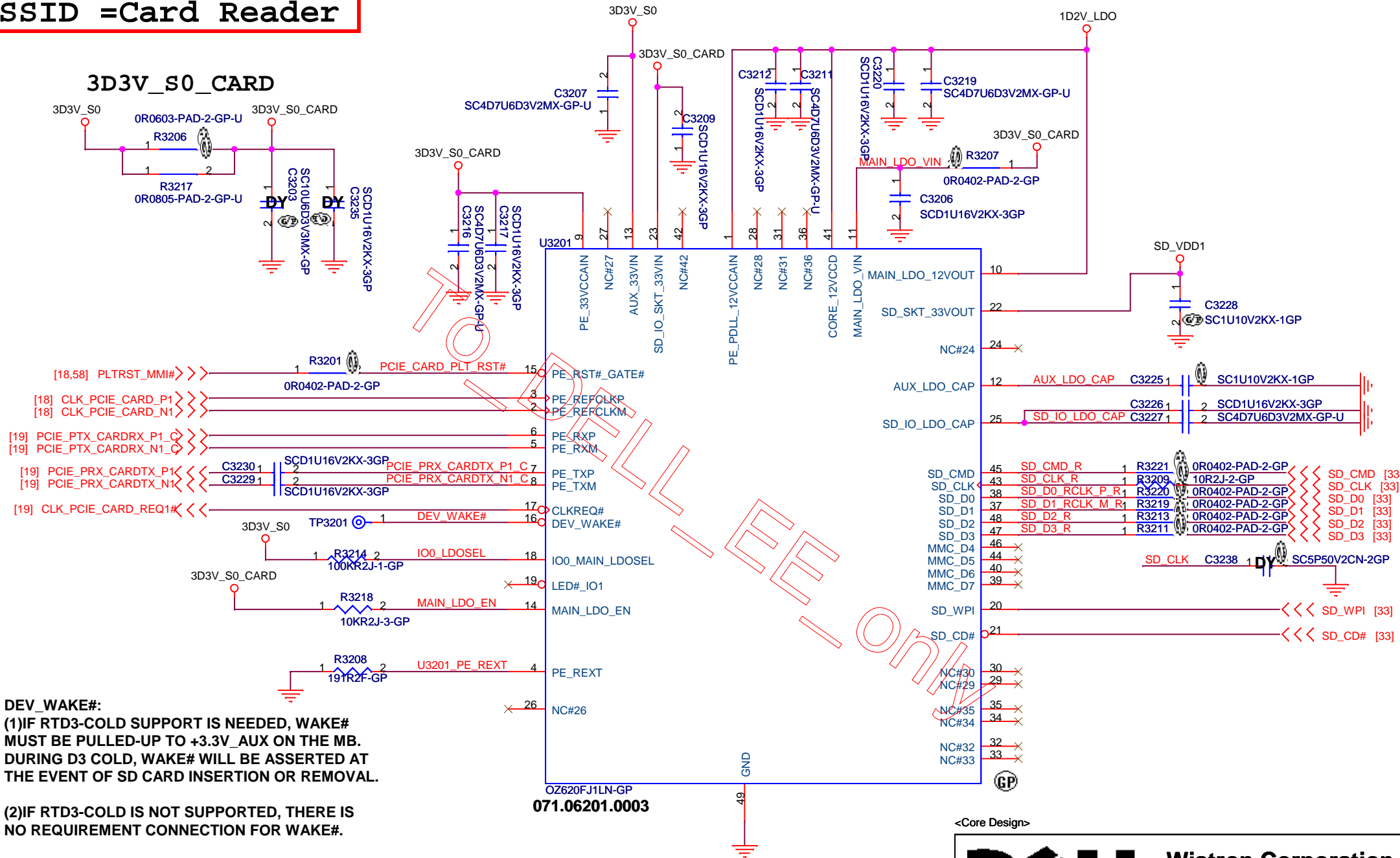
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 31 of 109

SSID =Card Reader



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Title

Card Reader

Size
A4

Document Number

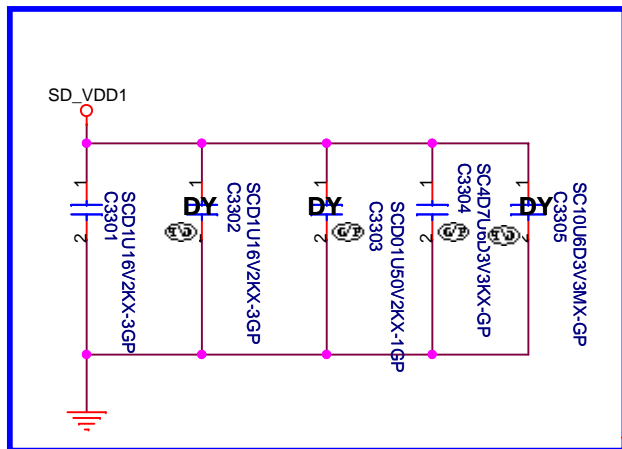
Plano 11.6" BTM

Rev
A00

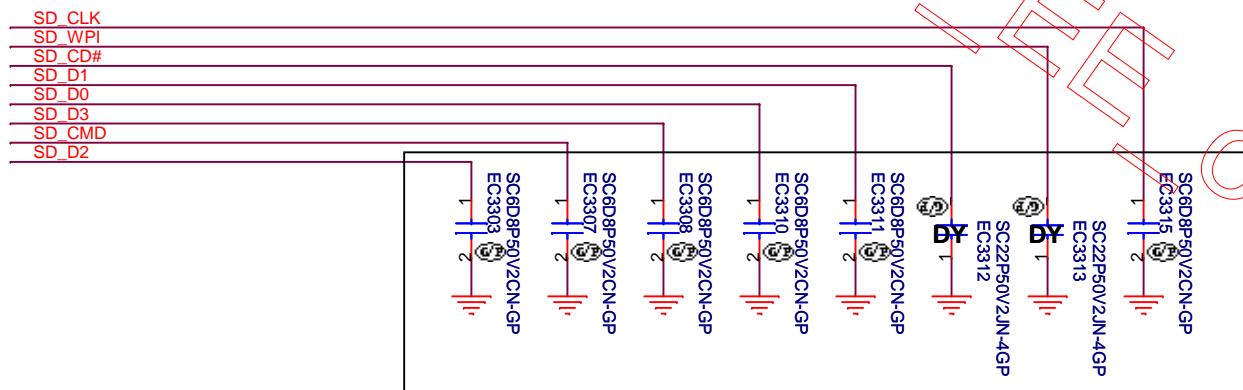
Date: Friday, December 19, 2014

Sheet 32 of 109

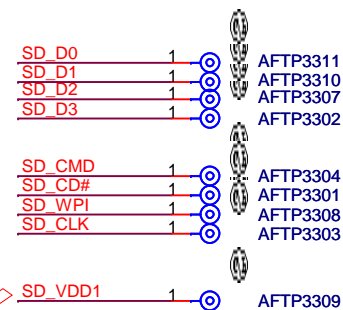
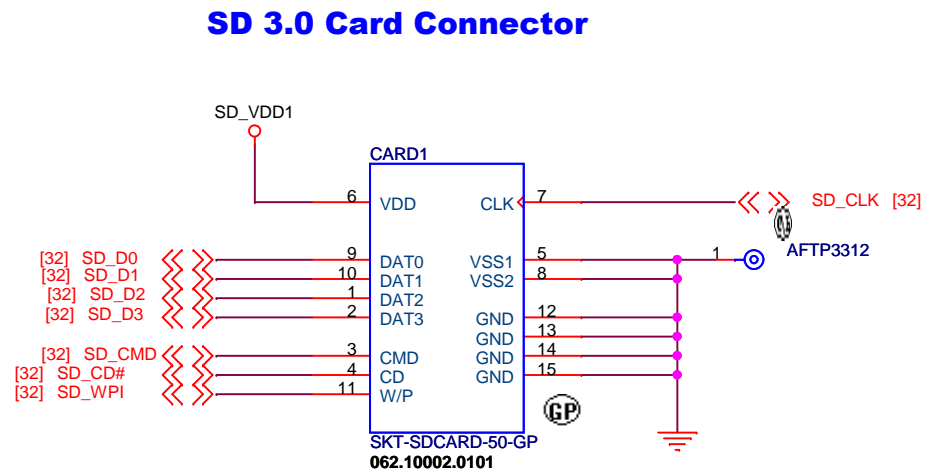
SSID =Card Reader



Layout Note:Close to Card Reader CONN

 $C \leq 10 \text{ pF}$

2014/10/30 DVT2 add cap for EMI



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Title

Card Reader CONNSize
A4

Document Number

Plano 11.6" BTM

Rev

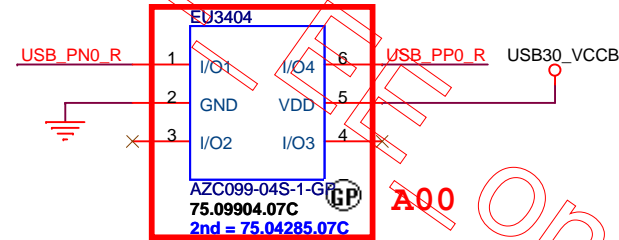
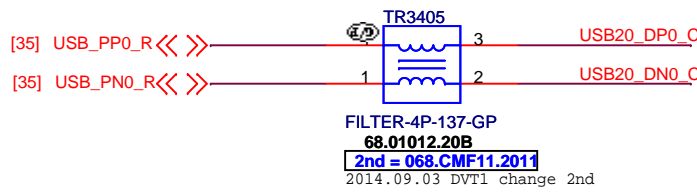
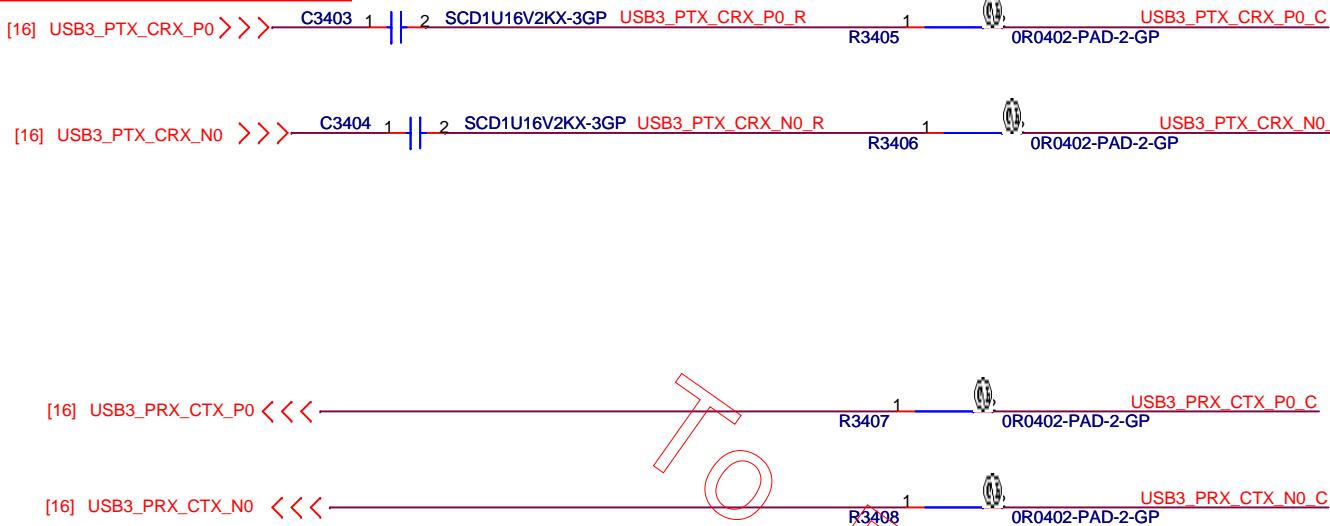
A00

Date: Tuesday, December 16, 2014

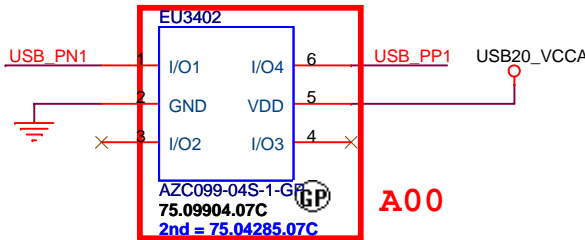
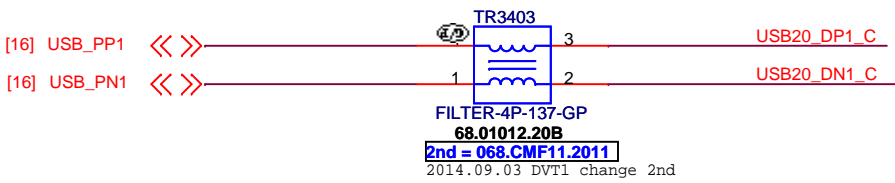
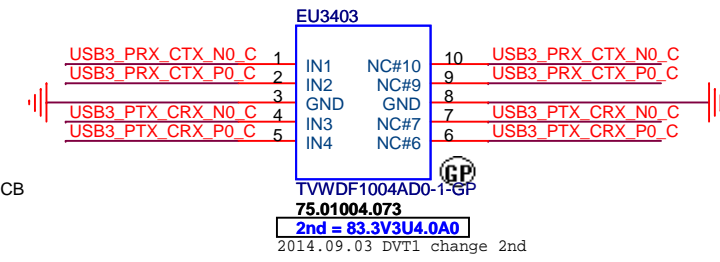
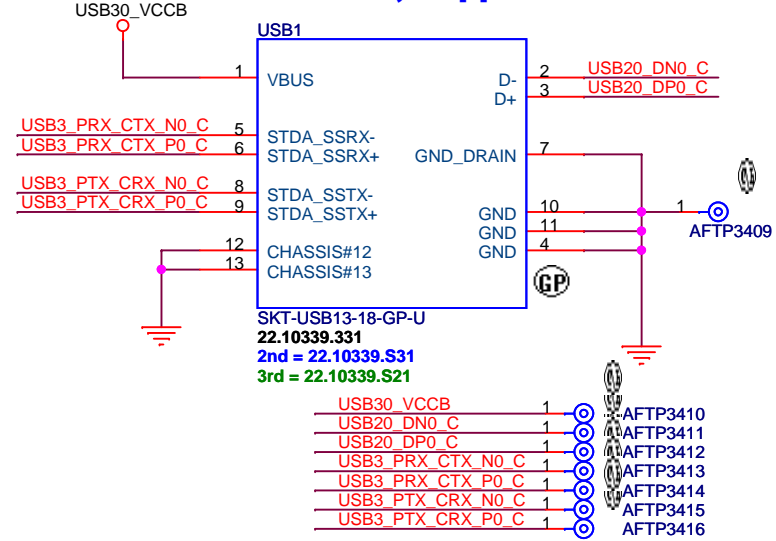
Sheet	33	of	109
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109

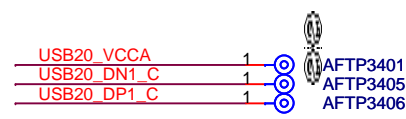
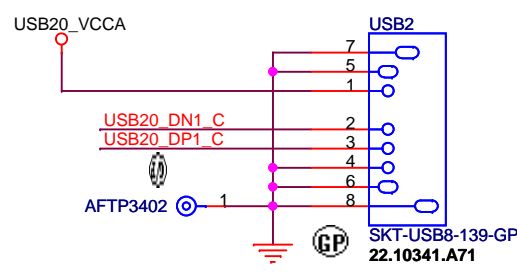
SSID = USB



EXT Port1 Left Side, Support Power Share



EXT Port2 Right Side

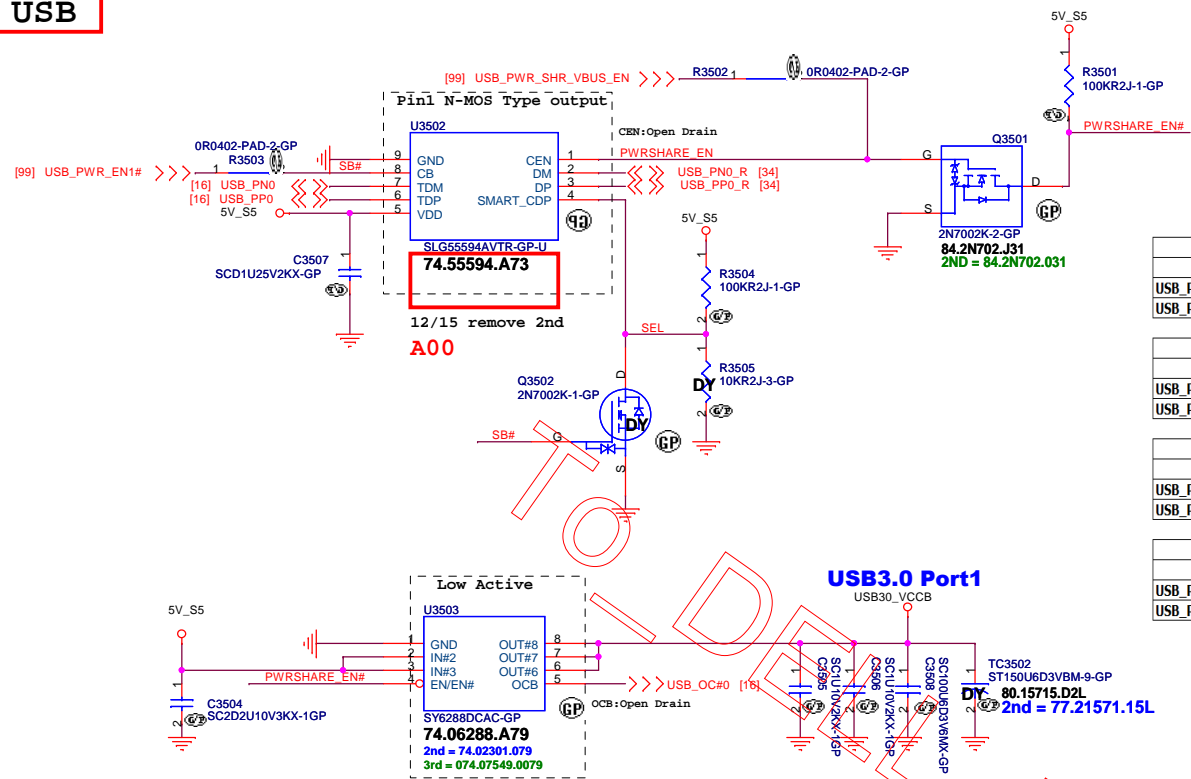


<Core Design>



Title		USB2.0/3.0/USBHubCONN	
Size	Document Number	Rev	
A4	Plano 11.6" BTM	A00	
Date:	Monday, December 22, 2014	Sheet	34 of 109

SSID = USB



CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.

AC mode				
Feature Enable/USB wake Enable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	1	1

DC mode				
Feature Enable/USB wake Enable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Enable/USB wake Disable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	1	1

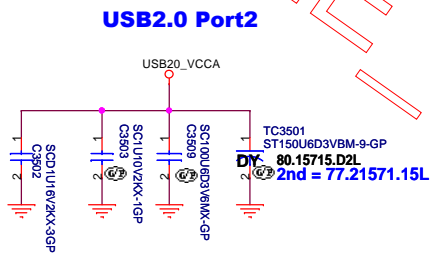
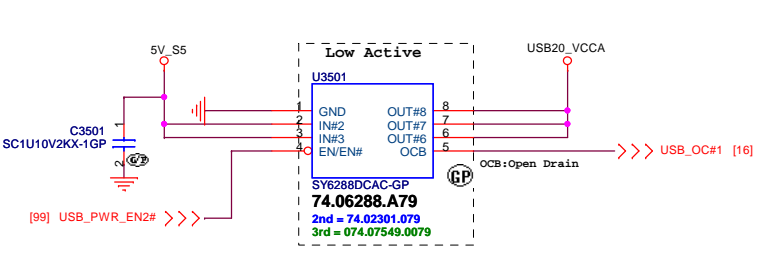
Feature Enable/USB wake Disable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Disable/USB wake Enable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Disable/USB wake Enable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	1	0	0

Feature Disable/USB wake Diable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	0	0	0

Feature Disable/USB wake Diable				
S0	S3	S4	S5	
USB_PWR_EN1# (Data)	1	0	0	0
USB_PWR_SHR_VBUS_EN (Charge)	1	0	0	0



USB Power SW (U3501 & U3503)


Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND

SSID = Reset.Suspend

(Blanking)

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Title <i>RUN POWER</i>		
Size A4	Document Number <i>Plano 11.6" BTM</i>	Rev <i>A00</i>
Date: Tuesday, December 16, 2014		Sheet 37 of 109

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Size
A4

Document Number

Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 38 of 109

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Title Reserved			
Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 39 of	109

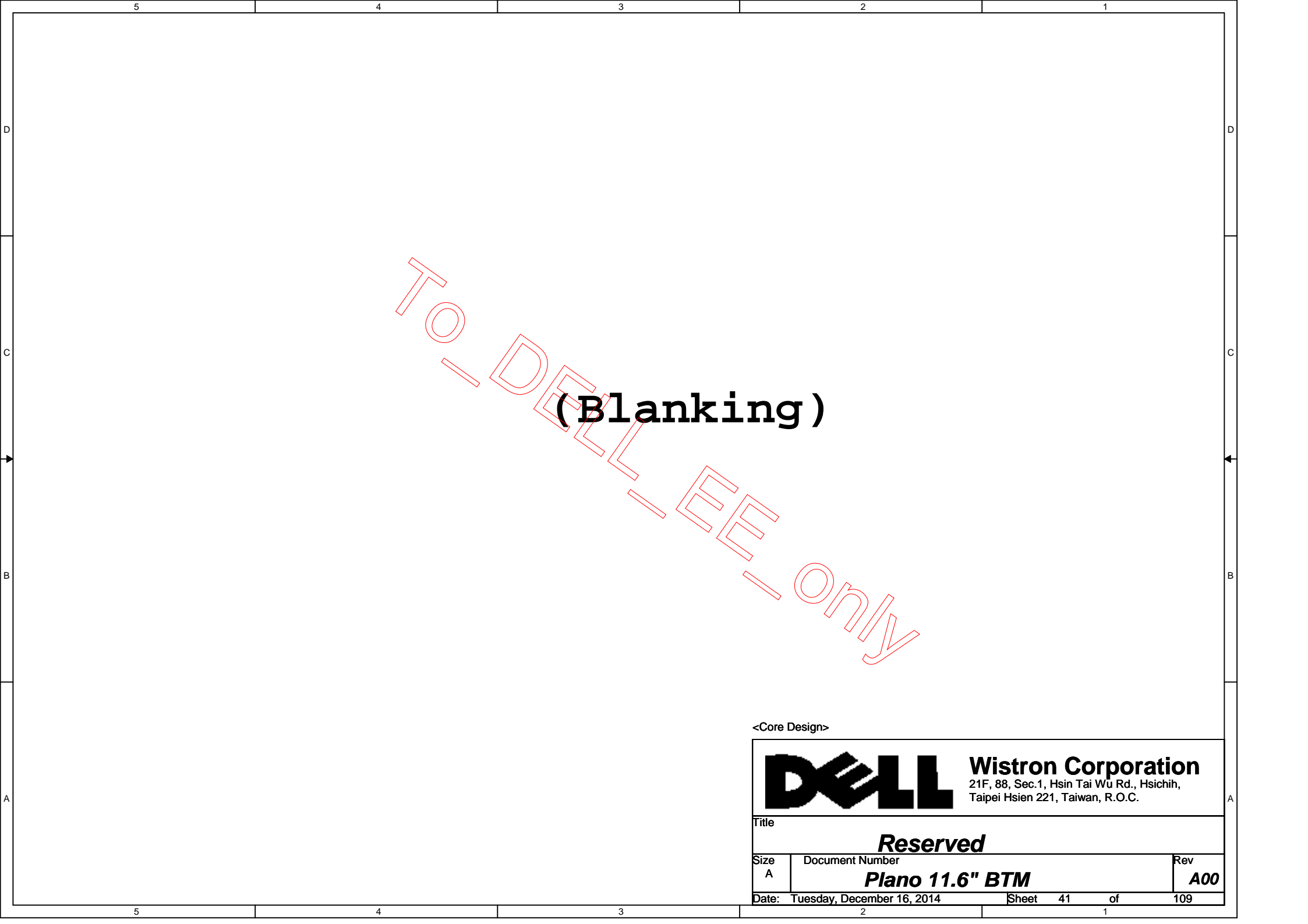
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Date: Tuesday, December 16, 2014		Sheet 40 of	109



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Rev

A00

Date: Tuesday, December 16, 2014

Sheet 41 of 109

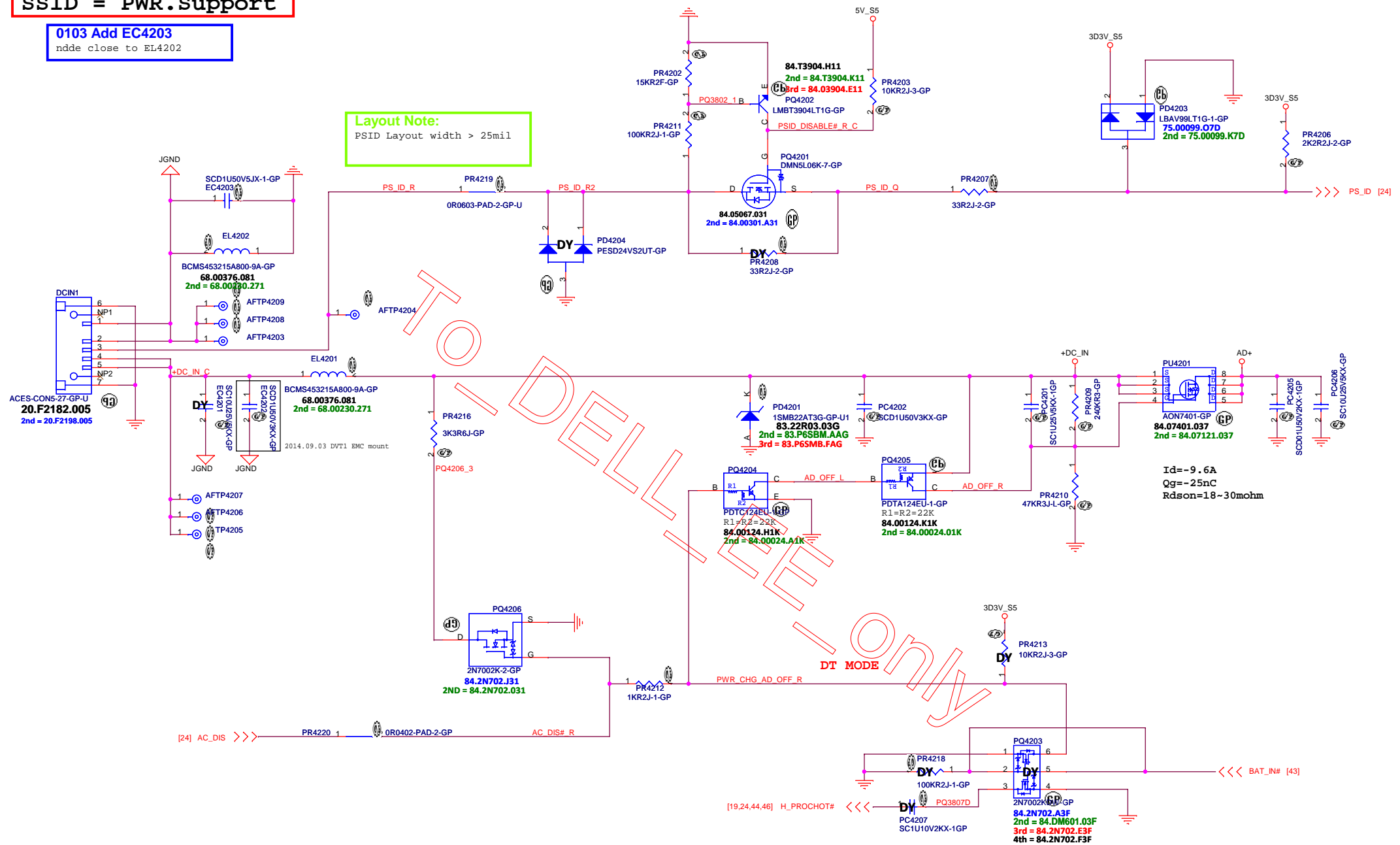
SSID = PWR.Support

0103 Add EC4203

ndde close to EL4202

Layout Note:

PSID Layout width > 25mil



<Core Design>



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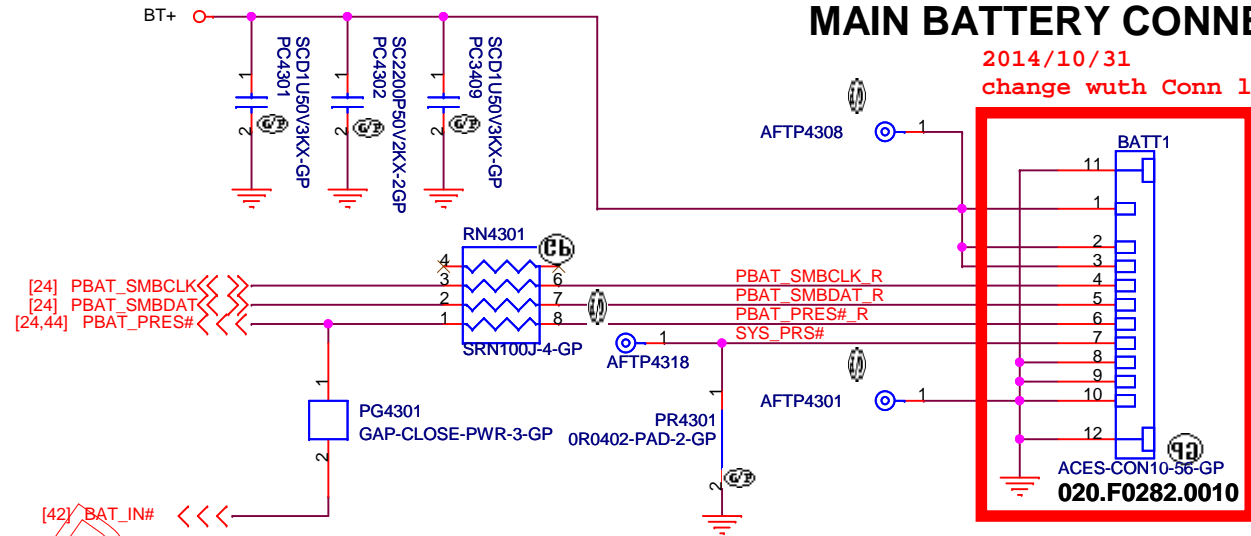
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Size A3	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014	Sheet 42 of 109	

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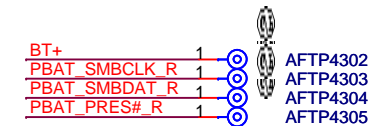
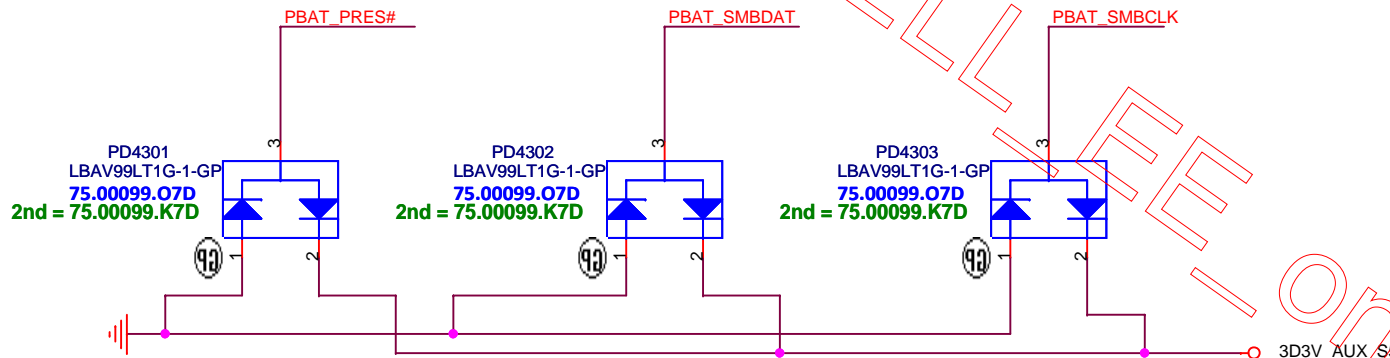
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MAIN BATTERY CONNECTOR

2014/10/31
change with Conn list X23



Layout Note: Place near Battery CONN



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BATTERY CONN

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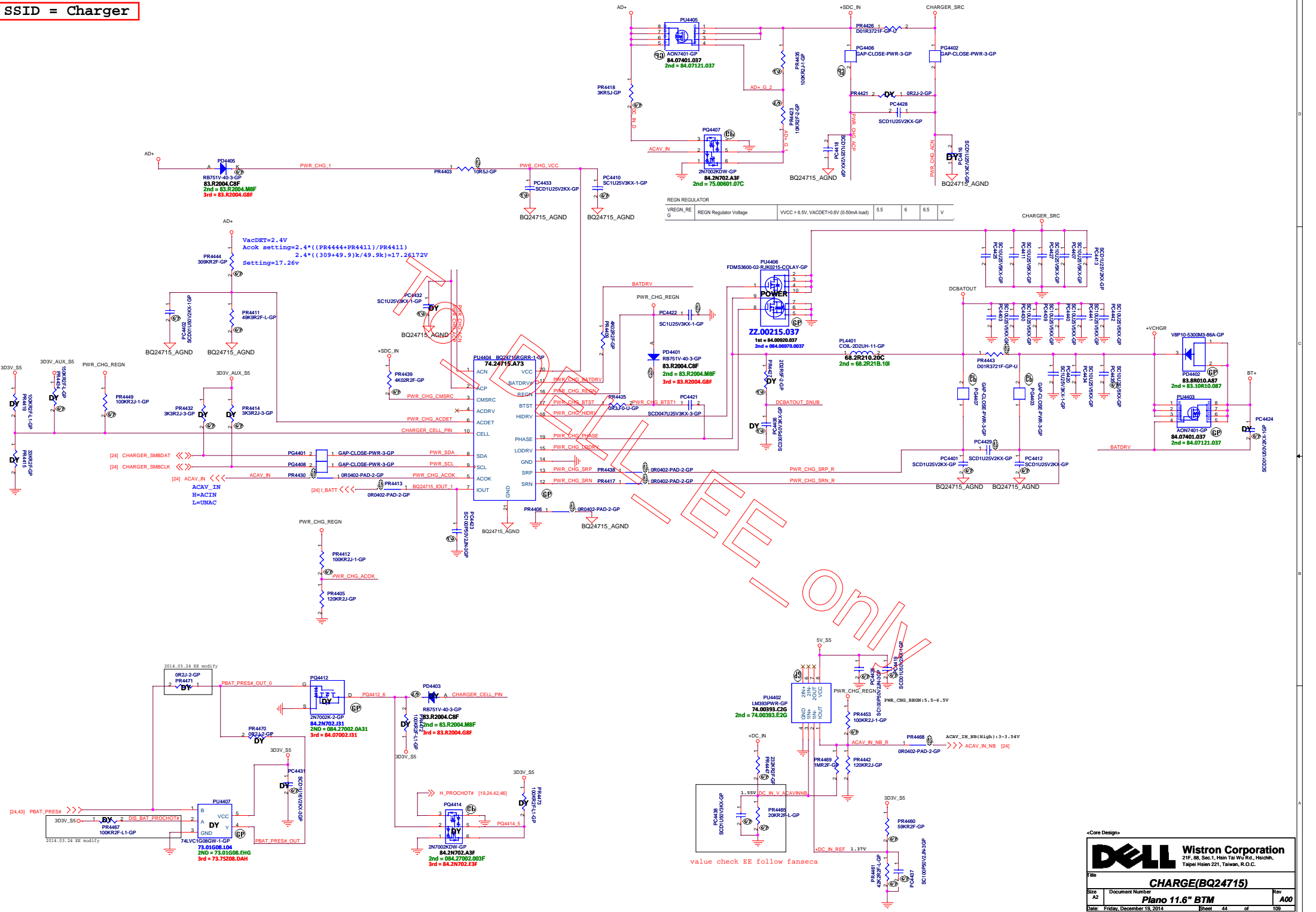
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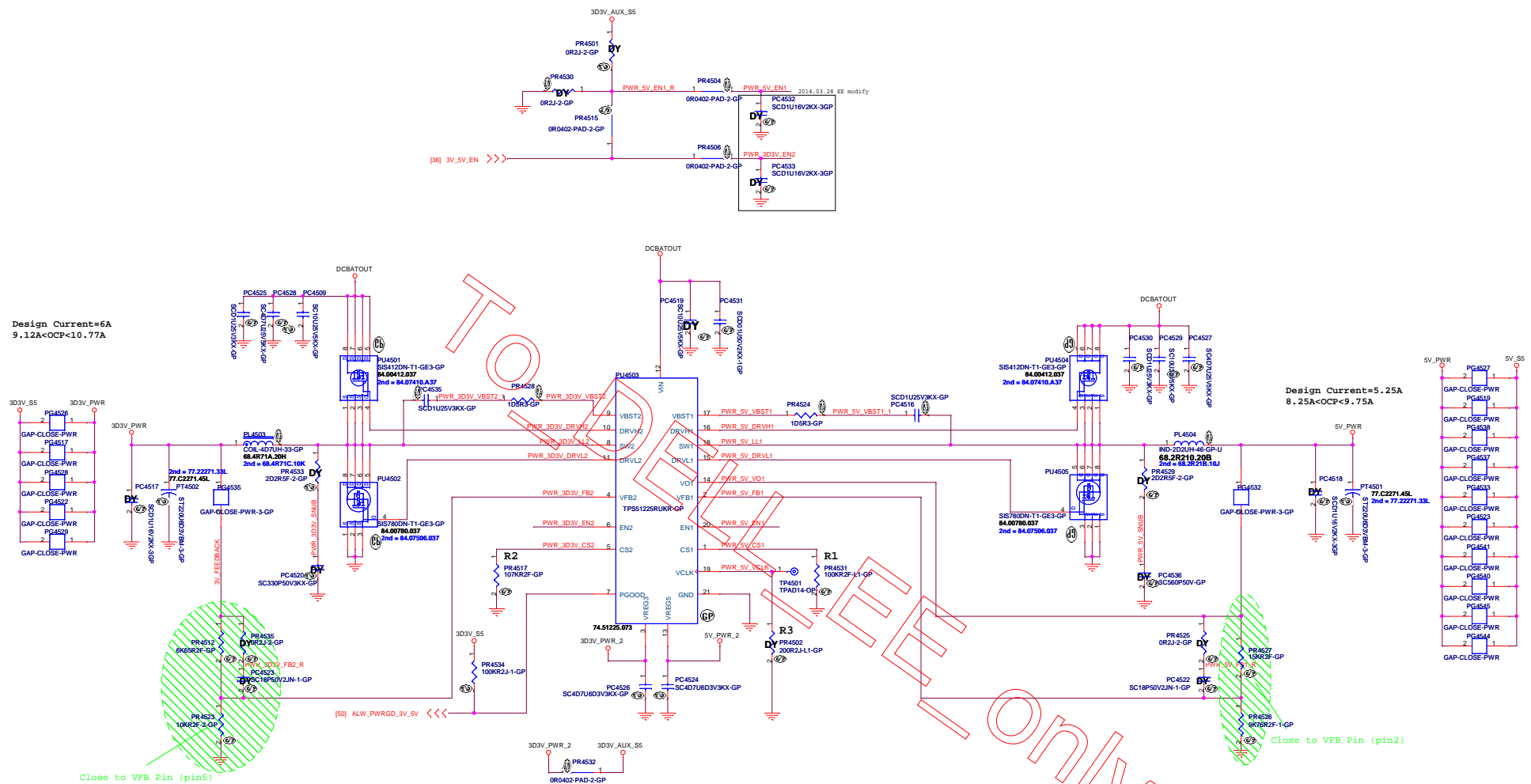
Date: Tuesday, December 16, 2014

Sheet 43 of 109

SSID = Charger



SSID = PWR.Plane.Regulator_5v3p3v

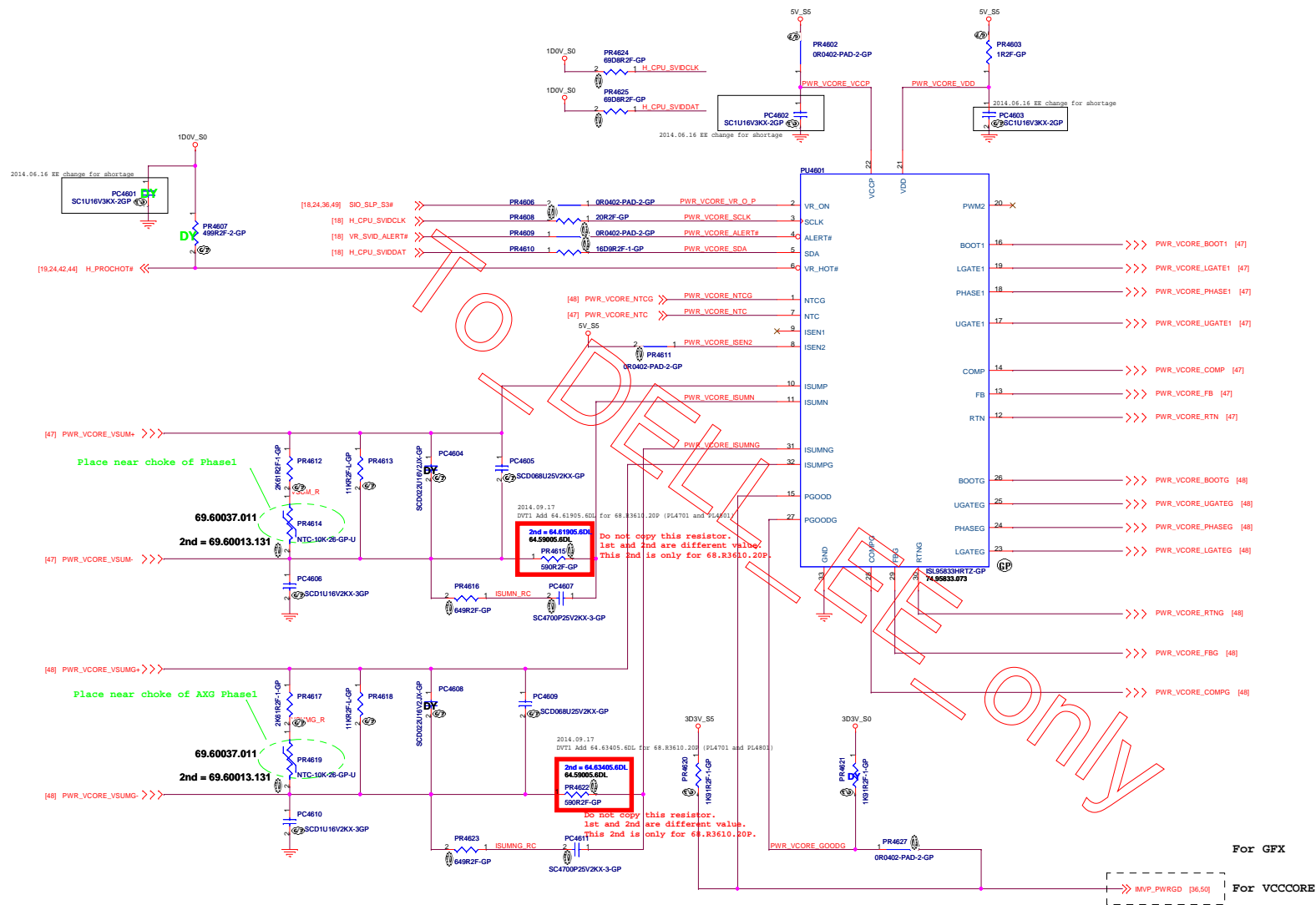


I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L
Inductor: CHIP CHOK 4.7UH PCMC063T-4R7MS Cynotec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

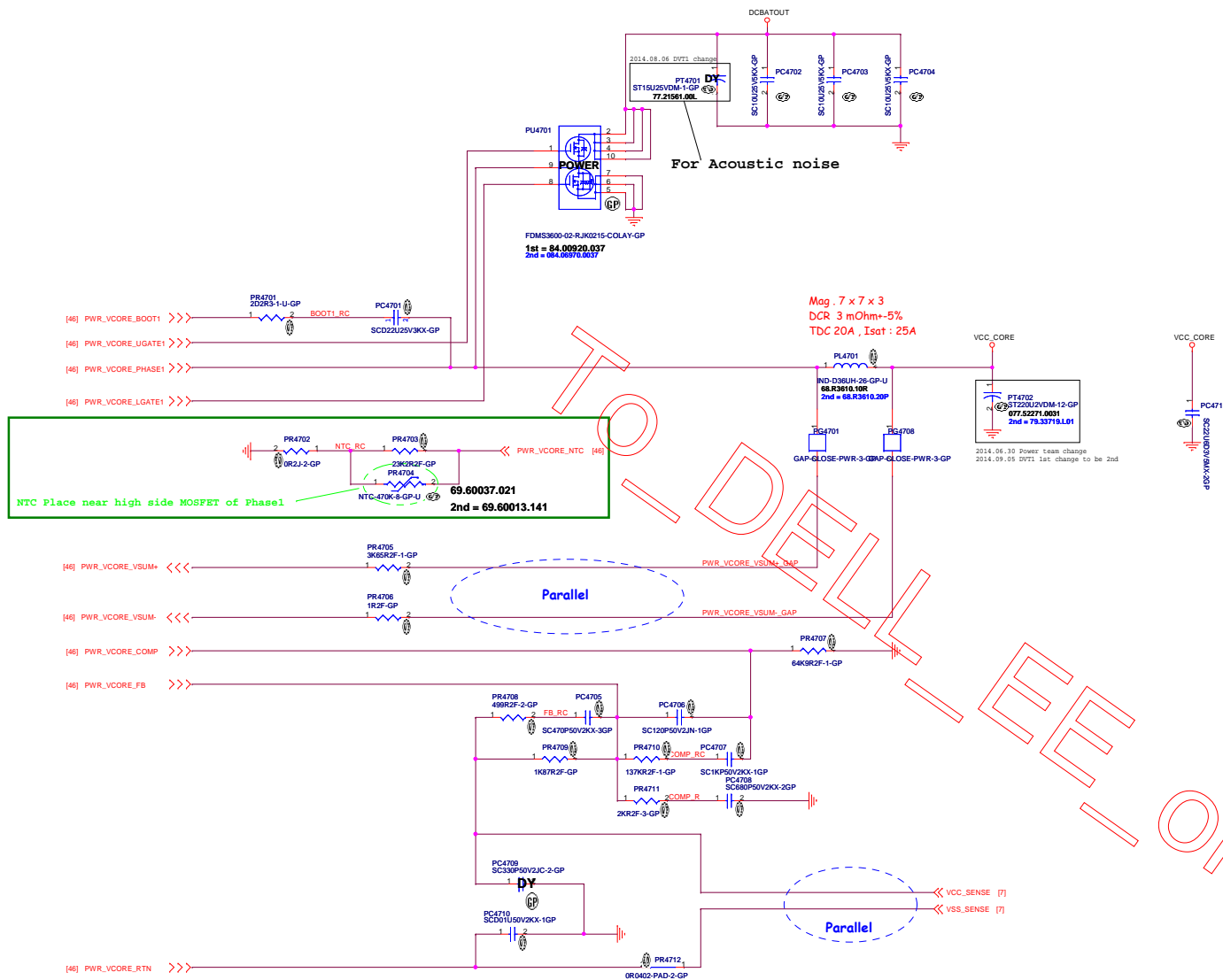
I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MNI 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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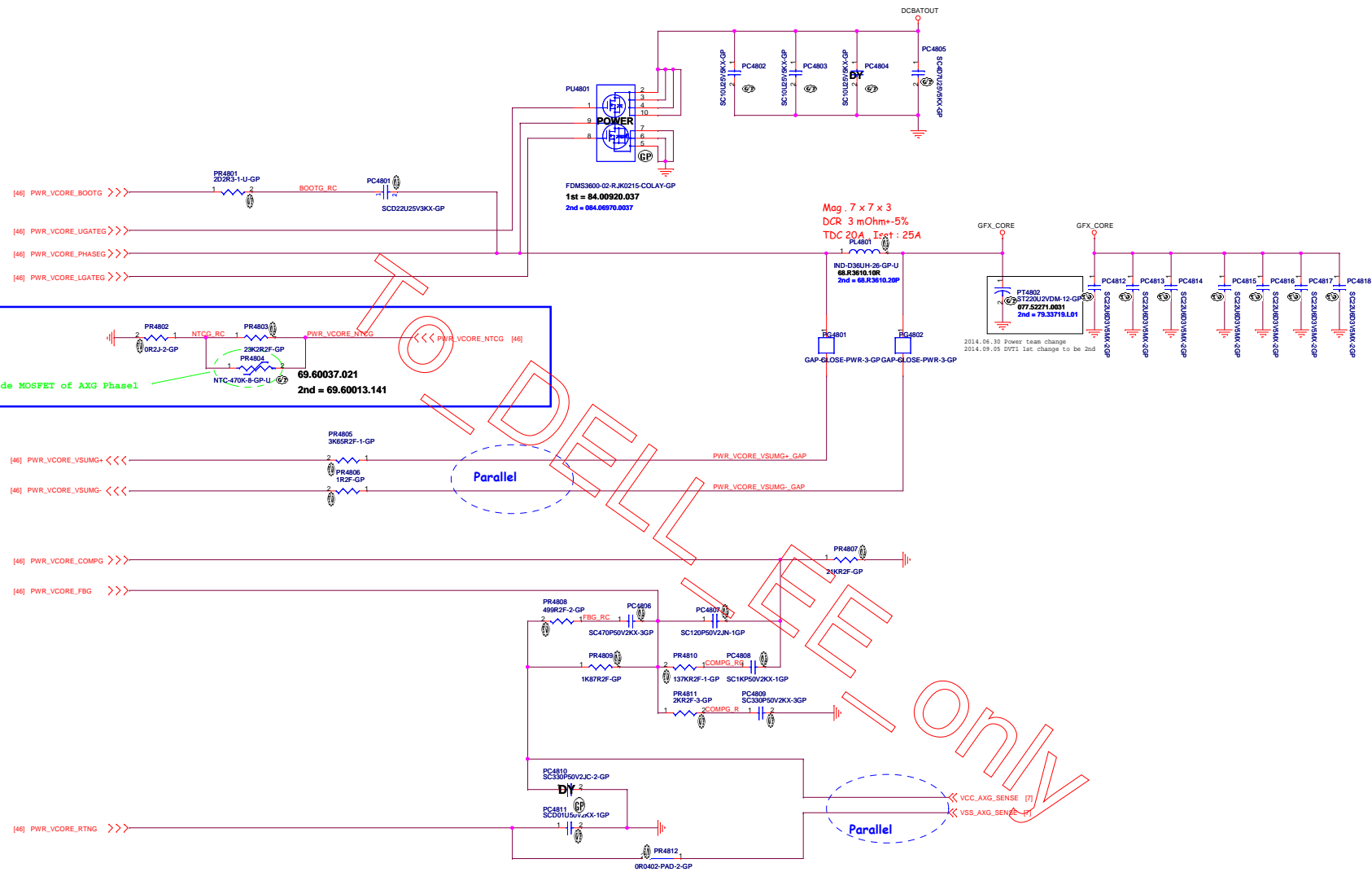
SSID = CPU Regulator



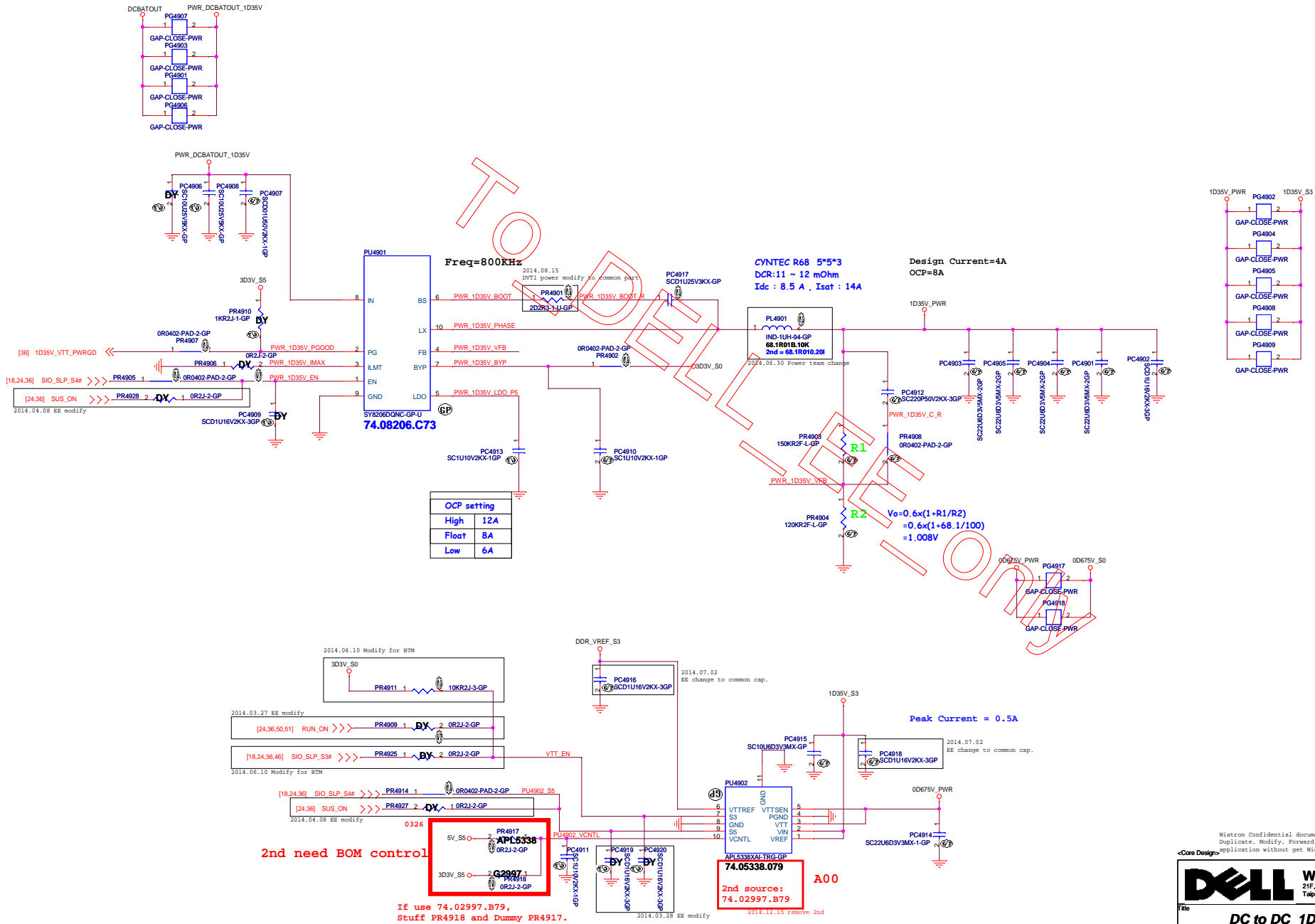
SSID = CPU Regulator



SSID = GFX Regulator



SY8206D for 1D35V



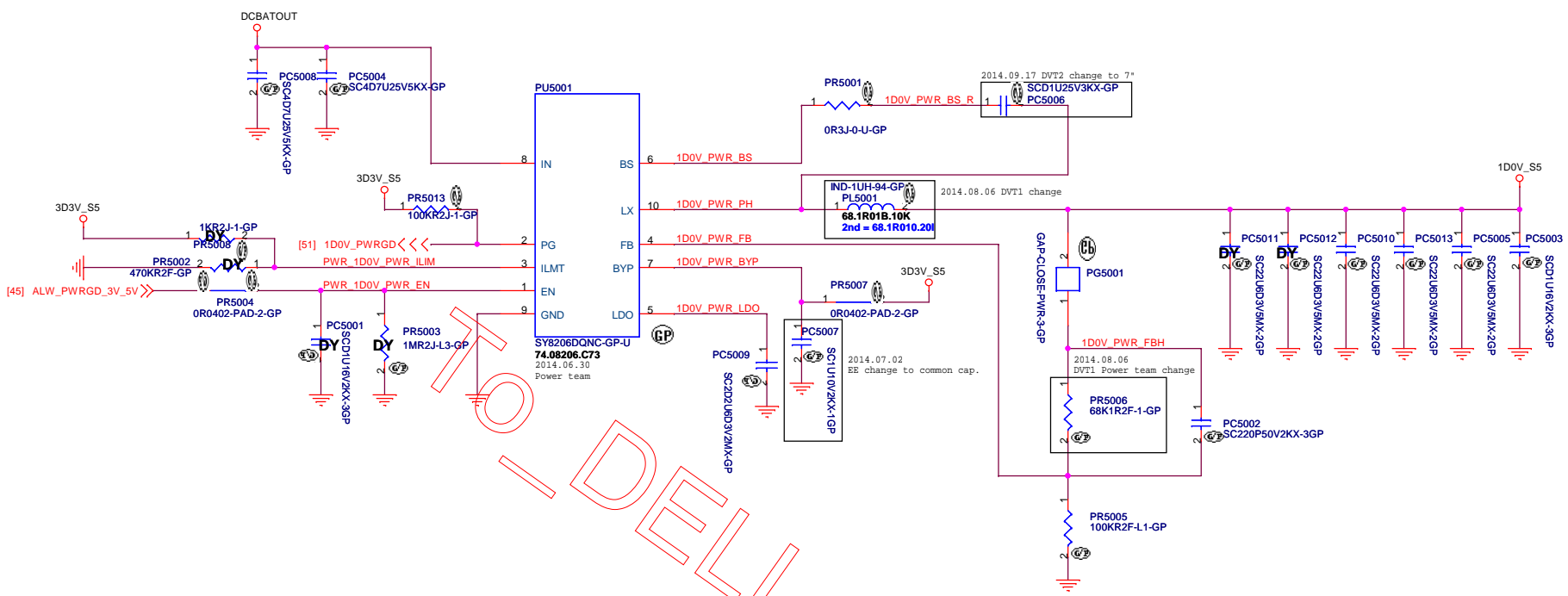
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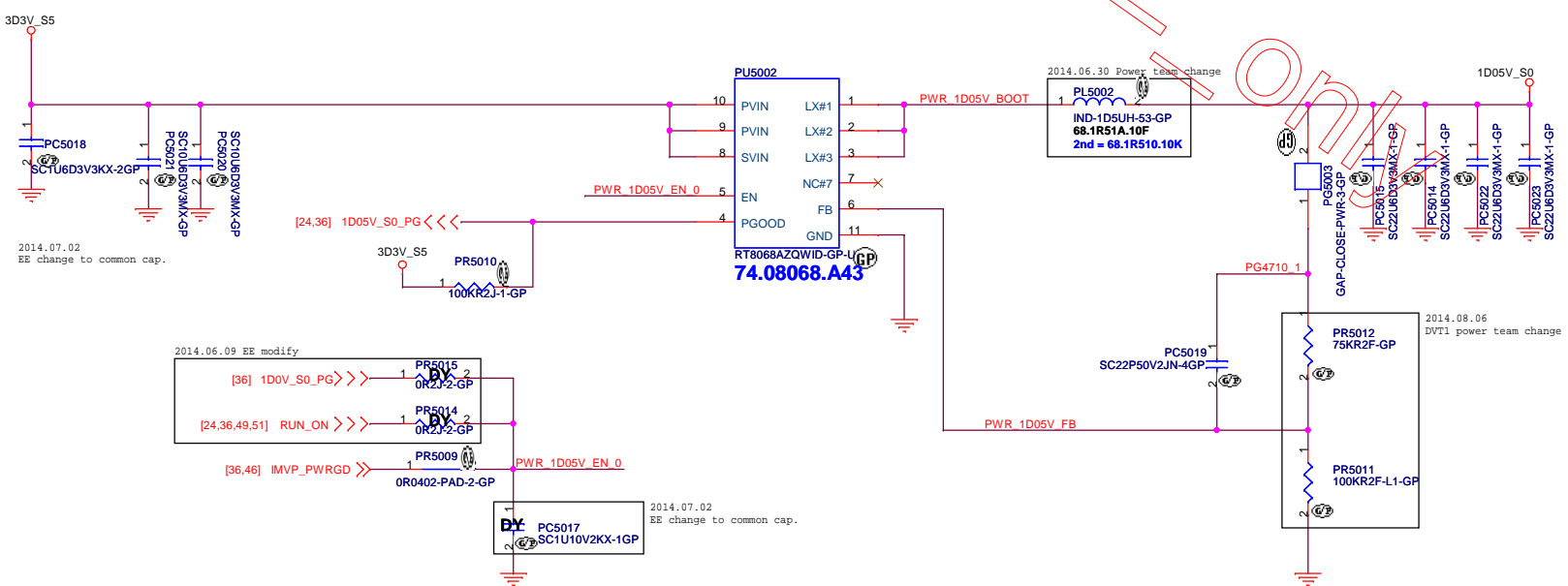
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DC to DC 1D35V(SY8208D)			
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Date	Issued	Sheet	of
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SSID = PWR.Plane.Regulator_1p05v

SY8206D for 1D0V_S5



RT8068 for 1D05V_S0



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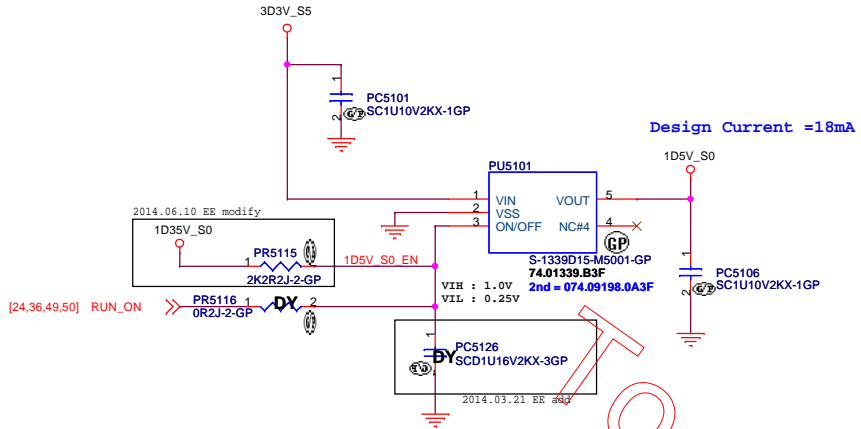
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Size: A3	Document Number: Plano 11.6" BTM	Rev: A00
Date: Tuesday, December 16, 2014	Sheet: 50	of: 109

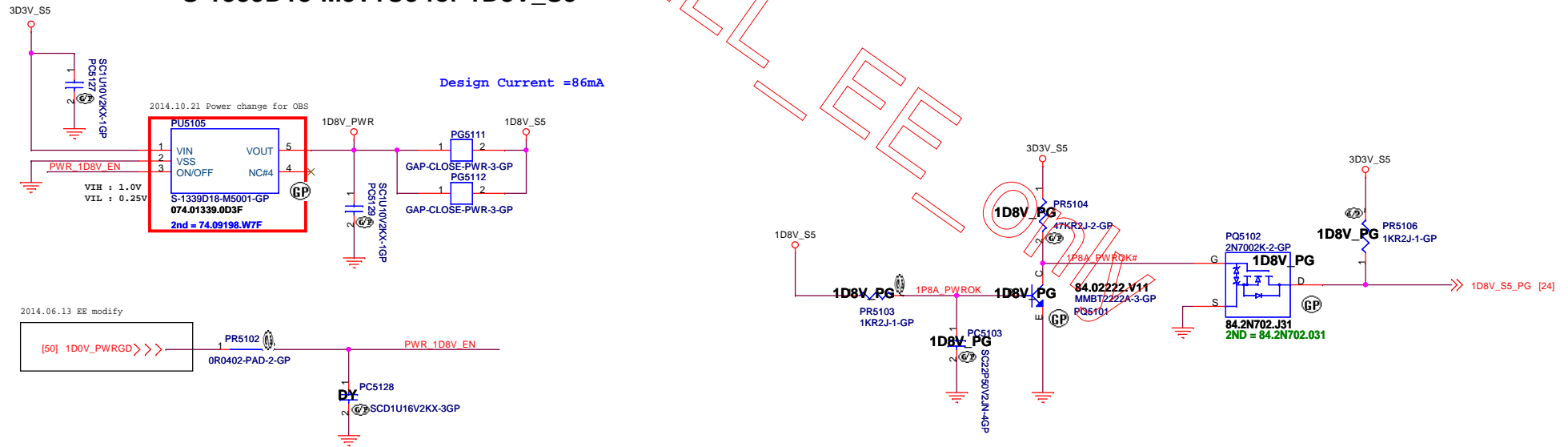
```
SSID = PWR.Plane.Regulator_1p5v
```

S-1339D15-M5001 for 1D5V_S0



```
SSID = PWR.Plane.Regulator_1p8v
```

S-1339D18-M5T1U3 for 1D8V_S5



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1D8V_1D5V

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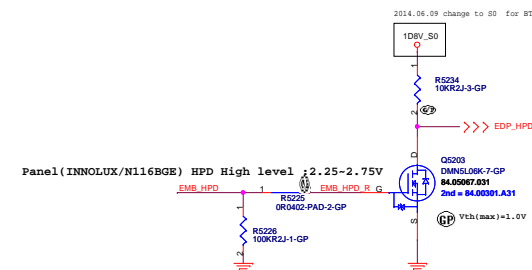
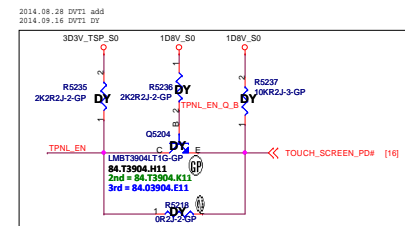
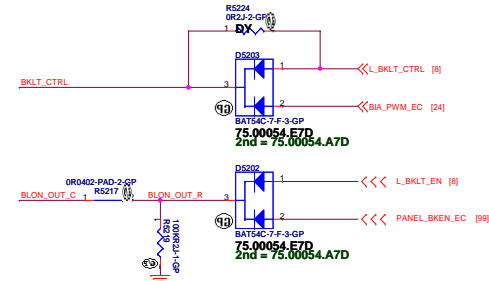
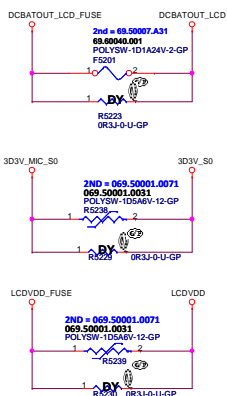
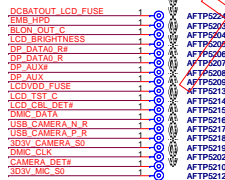
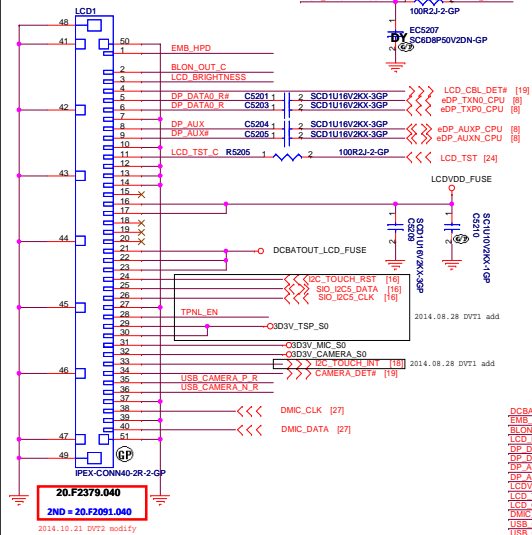
Rev

A00

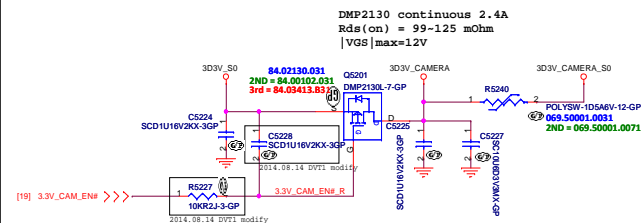
Date: Tuesday, December 16, 2014

Sheet	51	of	109
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eDP CONNECTOR

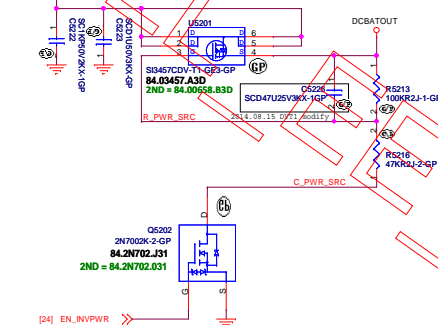


Camera Power



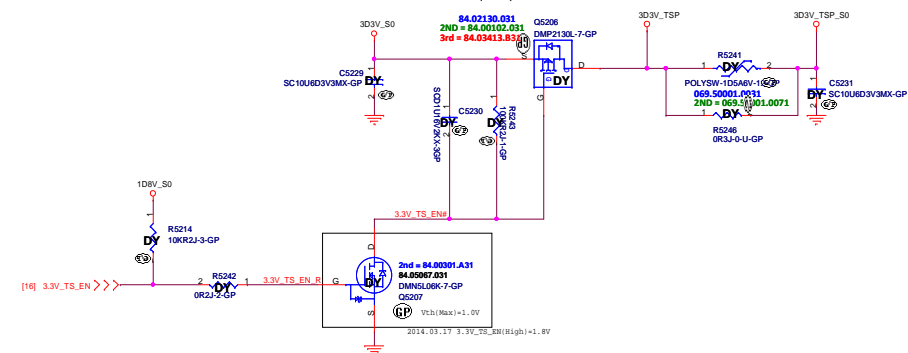
INVERTER POWER

SI3457 continuous 2.5A
Rds(on) = 0.113-0.092 Ohm
|VGS|max=20V



TOUCH PANEL POWER

DMP2130 continuous 2.4A
Rds(on) = 99-125 mOhm
|VGS|max=12V



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File	Document Number	Rev
A2	Plano 11.6" BTM	A00
Date:	Friday, December 19, 2014	Sheet 52 of 109

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Document Number

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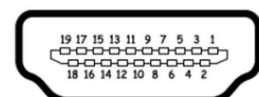
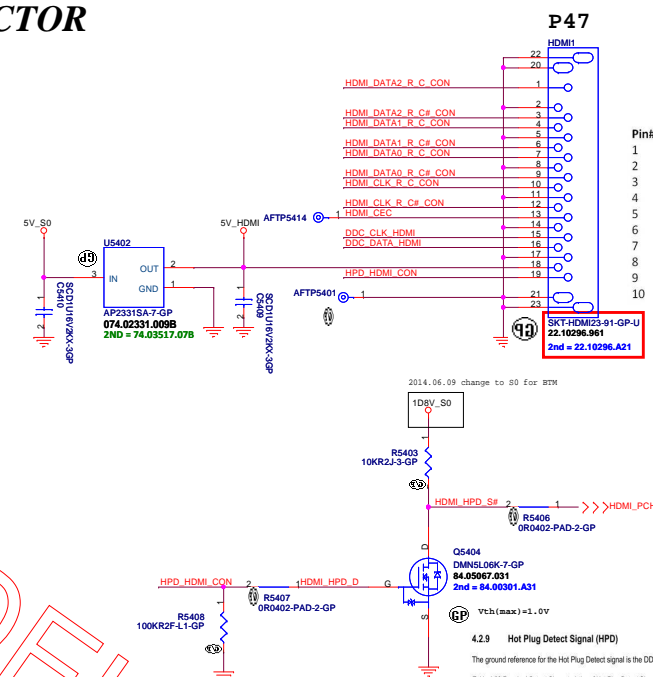
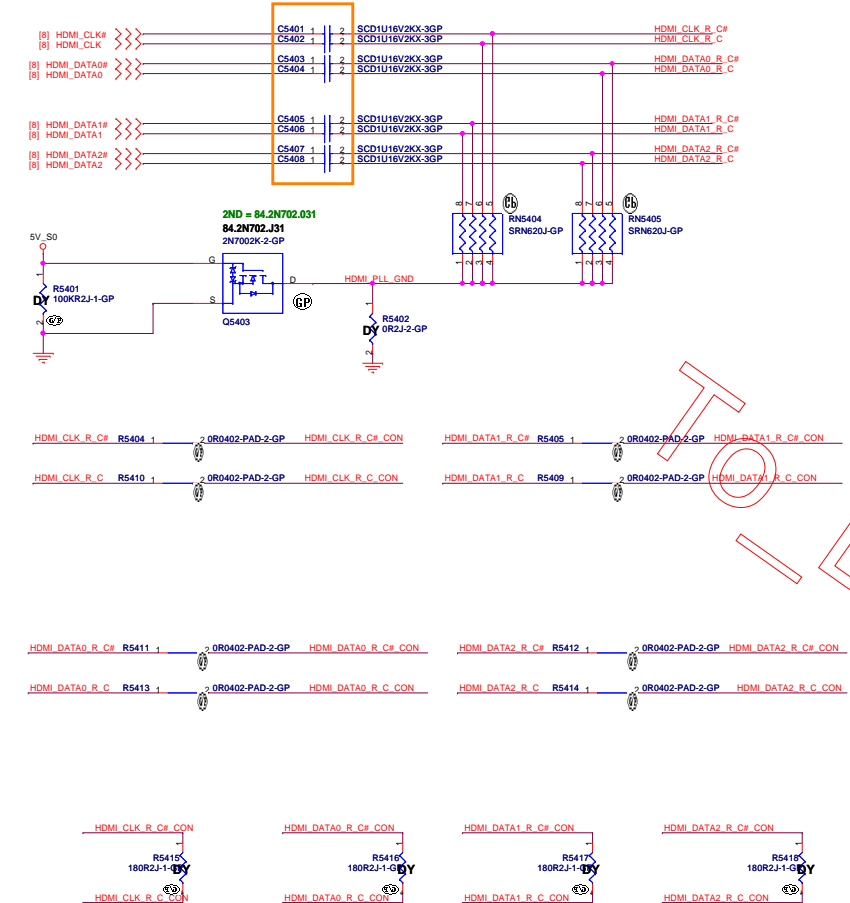
Rev
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Date: Tuesday, December 16, 2014

Sheet 53 of 109

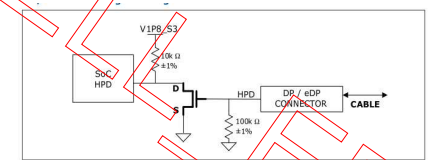
HDMI CONNECTOR

Close to HDMI Connector



Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		

A00



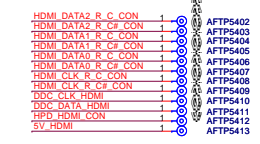
NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate-Threshold Voltage <= 1.5V.
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)
The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.
Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms <20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts



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HDMI Level Shifter/Connector

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Date: Thursday, December 25, 2014 Sheet: 54 of 109

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Title

HDMI Level Shifter/Connector

Size
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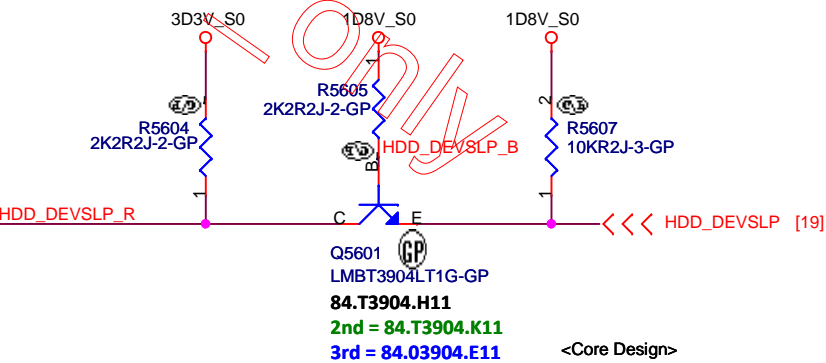
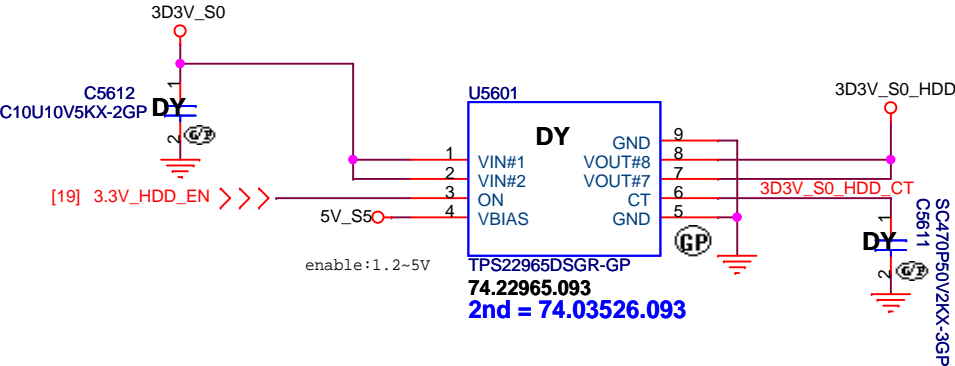
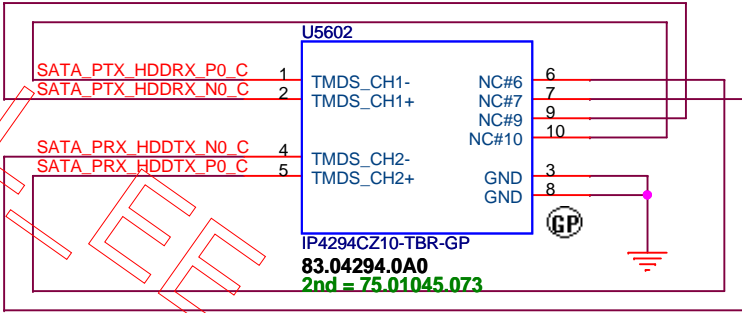
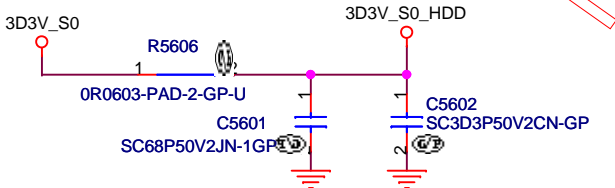
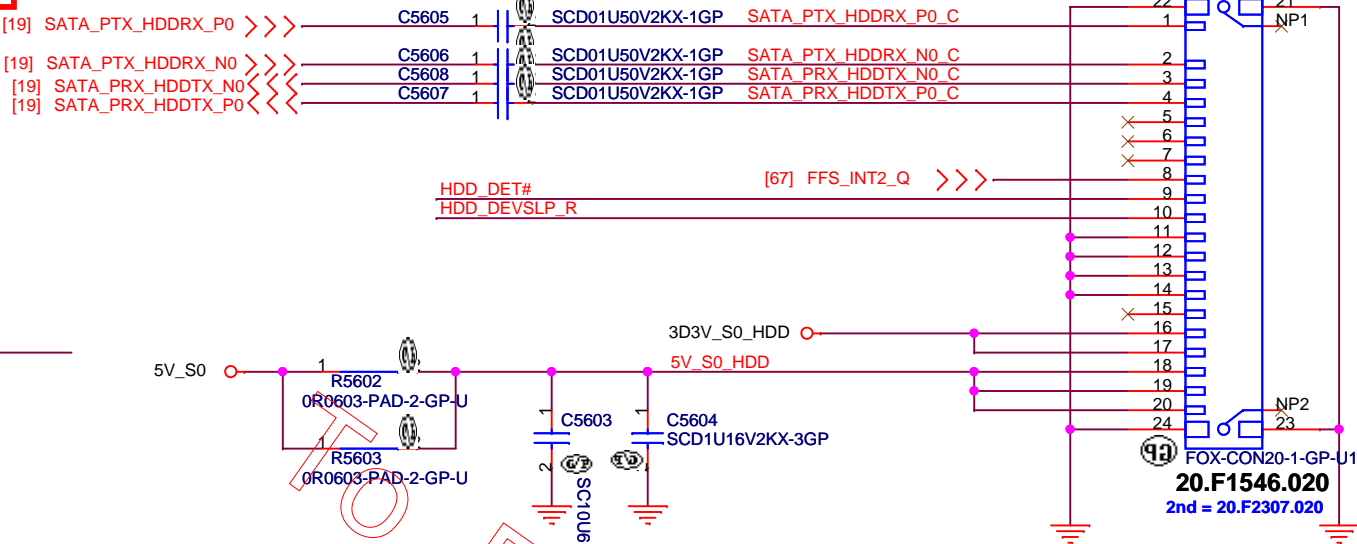
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A00

Date: Tuesday, December 16, 2014

Sheet 55 of 109

SSID = SATA




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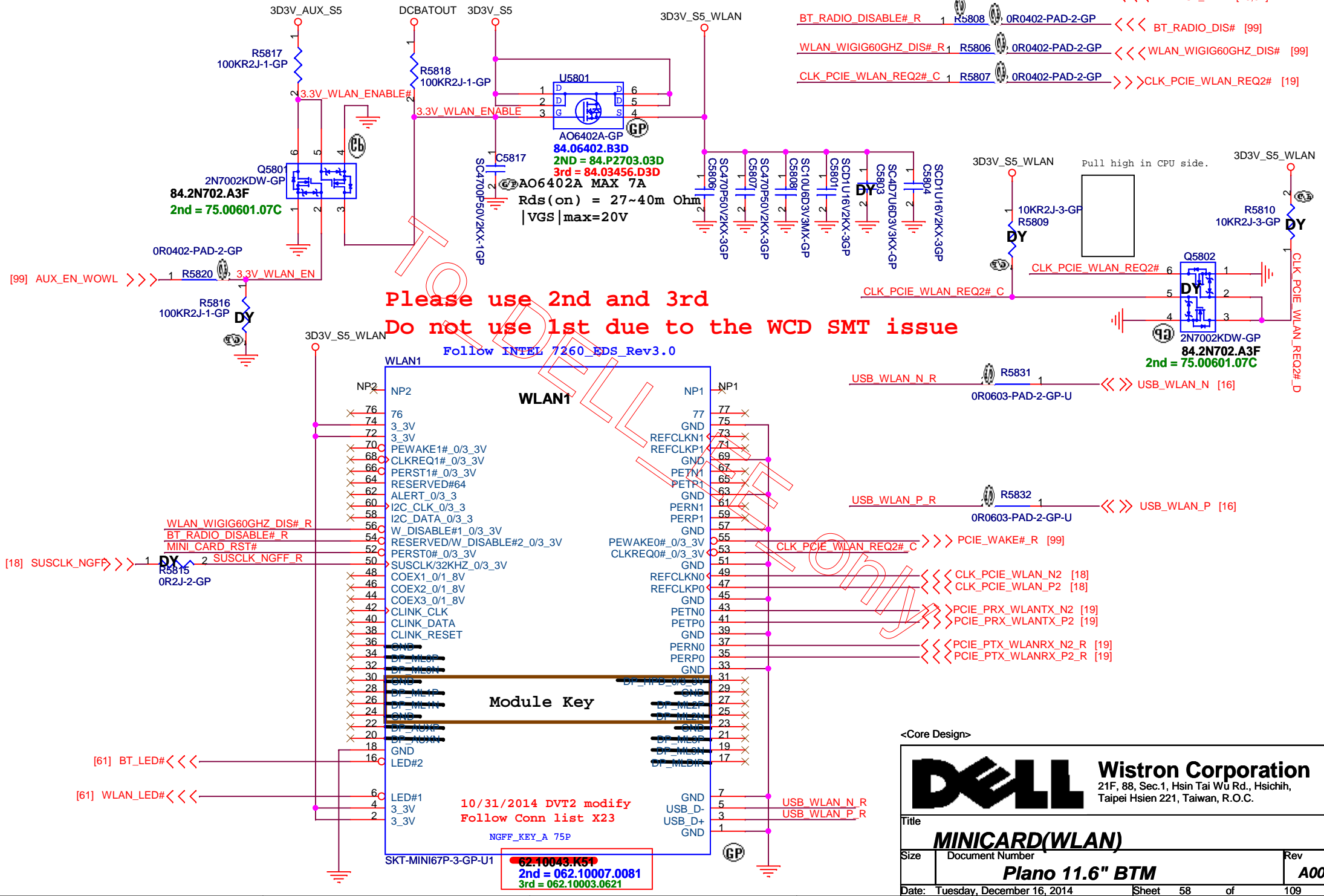
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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 57 of	109

SSID = WIRELESS



NGFF SSD




SSID =WIRELESS

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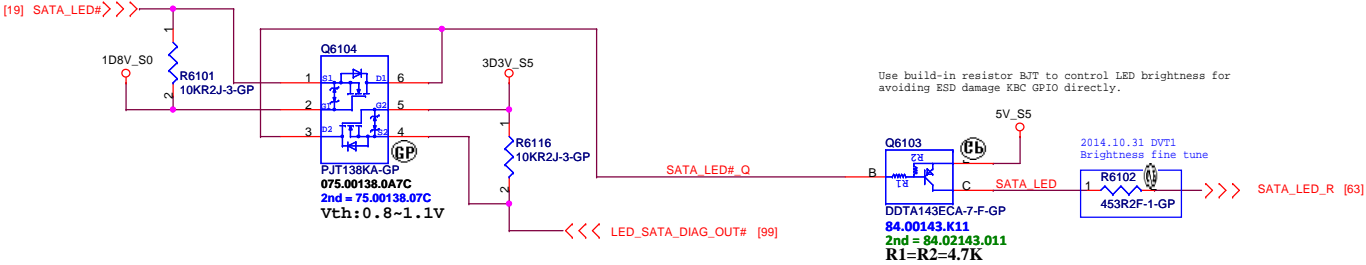
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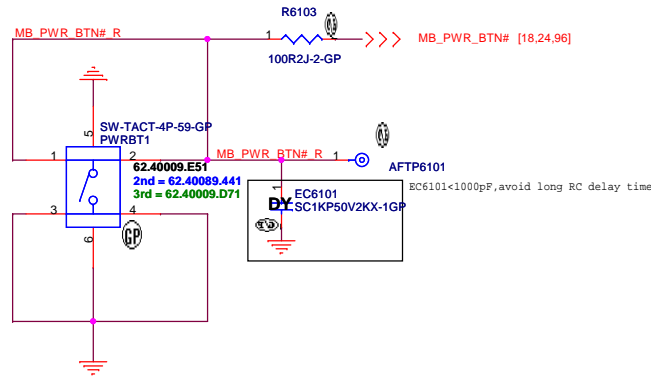
Date: Tuesday, December 16, 2014Sheet 60 of 109

SSID = User.Interface

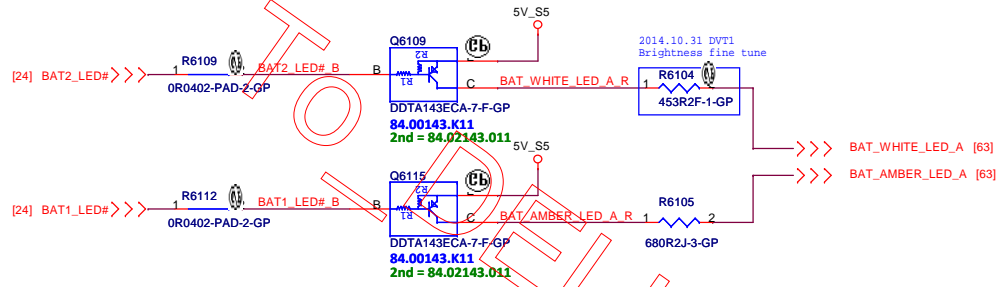
SATA HDD LED
LOW activated from PCH GPIO



POWER BUTTON

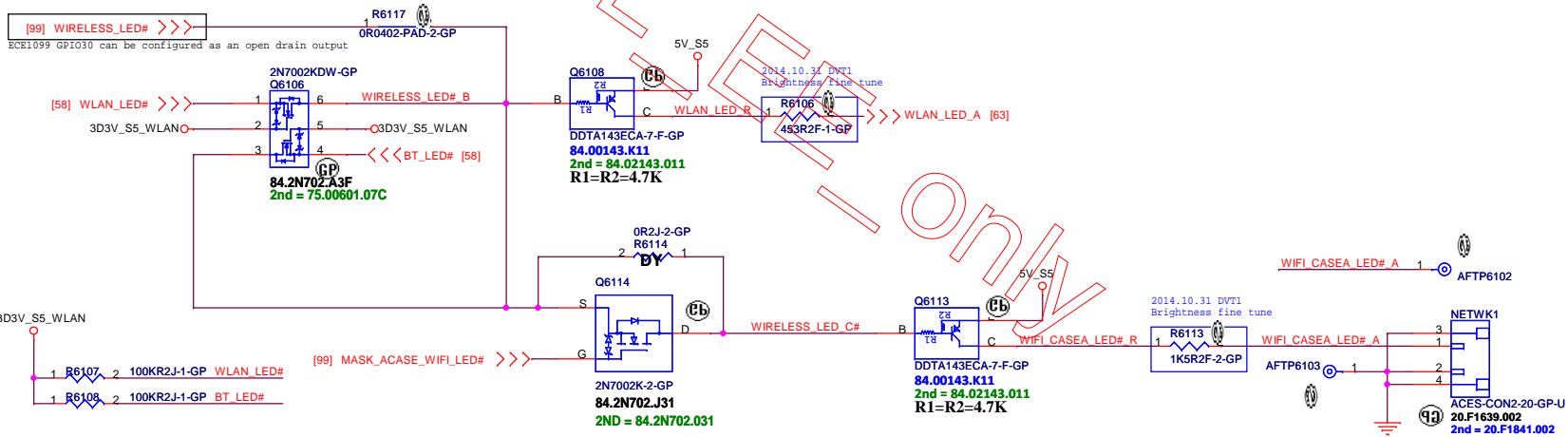


Battery LED2(White_LED)
LOW activated from KBC GPIO

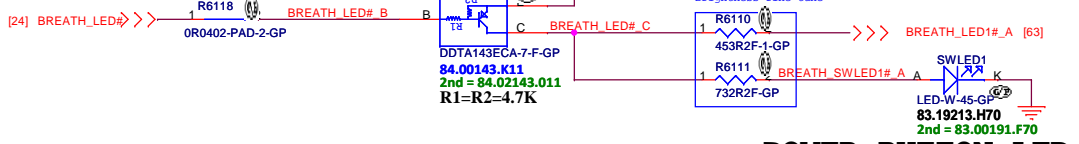


Battery LED1(Orange_LED)
LOW activated from KBC GPIO

WLAN LED
LOW activated from KBC GPIO



Power LED
LOW activated from KBC GPIO



POWER BUTTON LED

<Core Design>

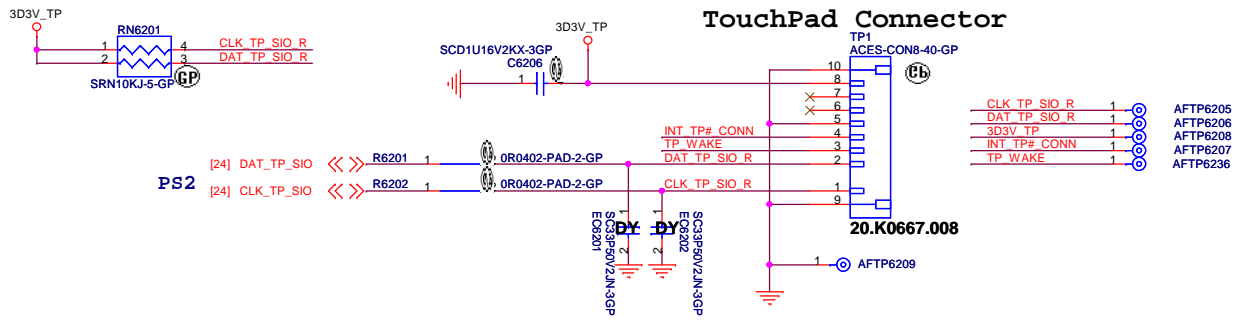
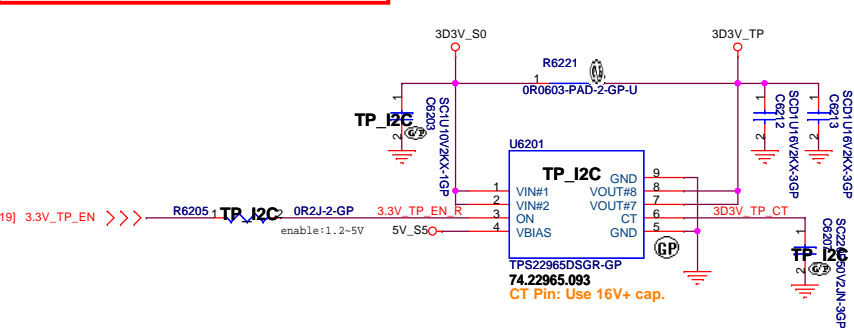
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Title **LED**

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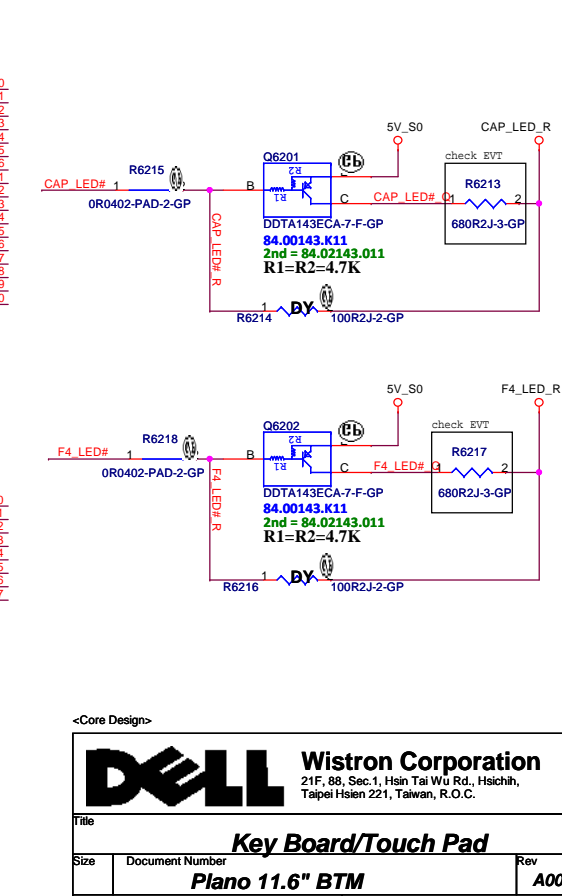
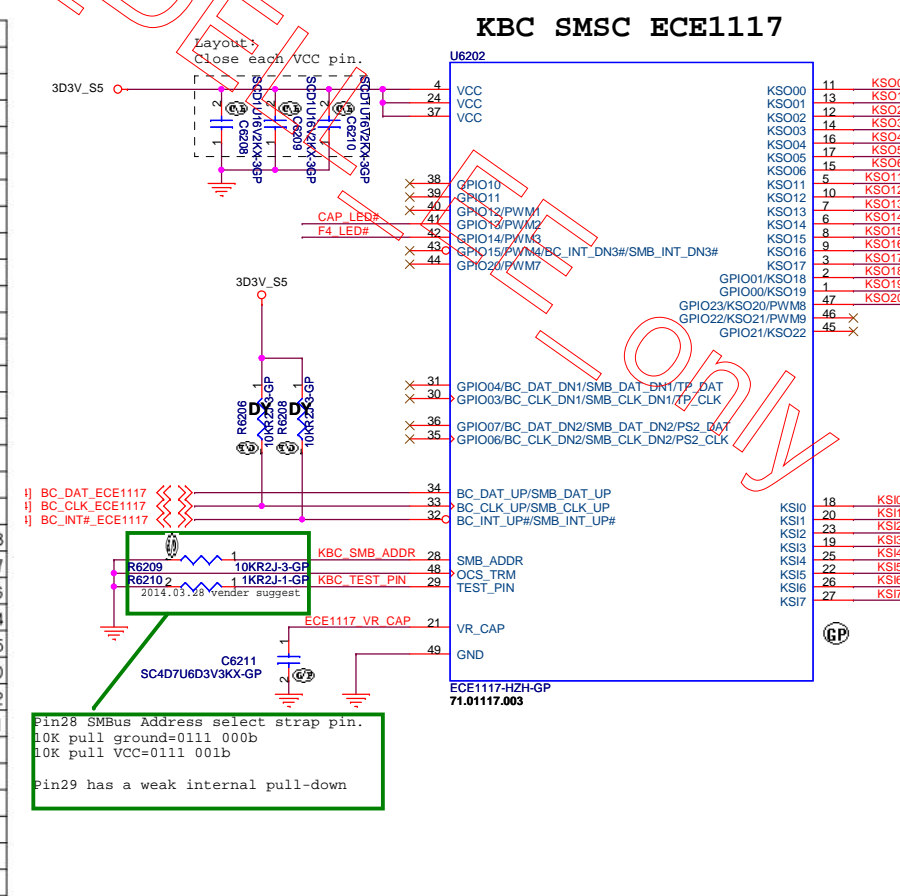
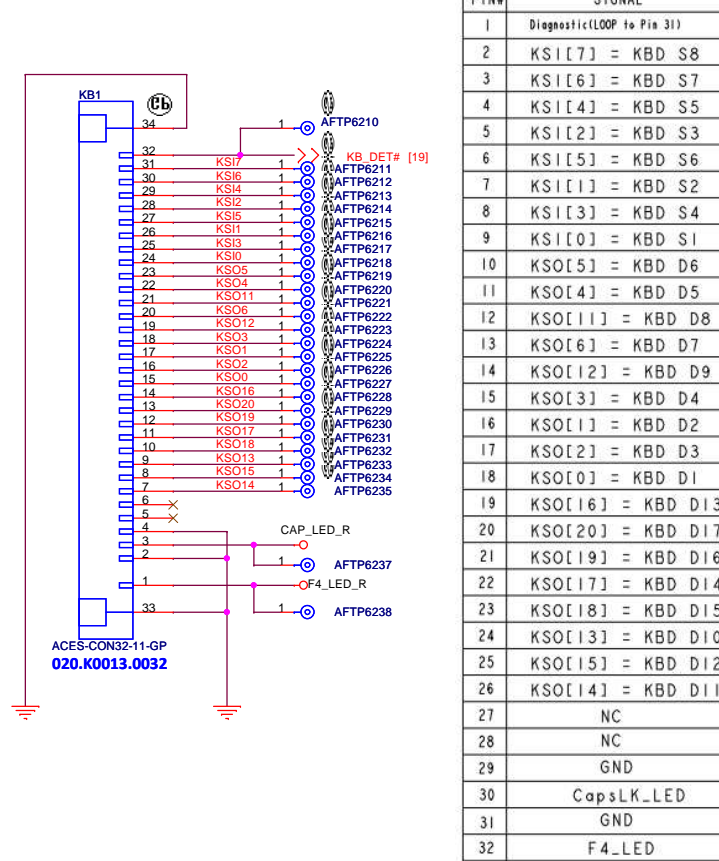
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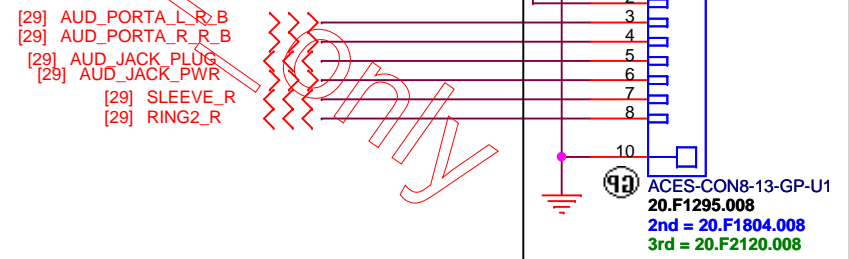
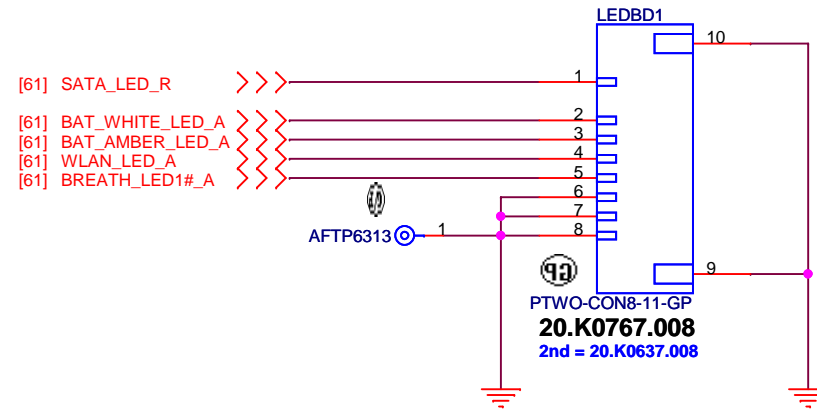
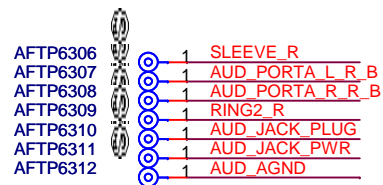
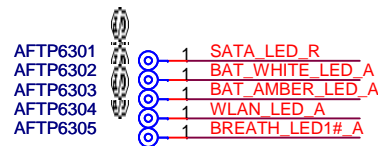
SSID = Touch.Pad



SSID = KBC

Internal KeyBoard Connec





2014.06.03 Modify pin assign for connector change

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Document Number

Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 63 of 109

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Hall Sensor

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Document Number

Plano 11.6" BTM

Rev

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Date: Tuesday, December 16, 2014


Sheet 64 of 109

SSID = DEBUG PORT

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Size	Document Number		Rev
	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014		Sheet 65 of 109

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SENSOR

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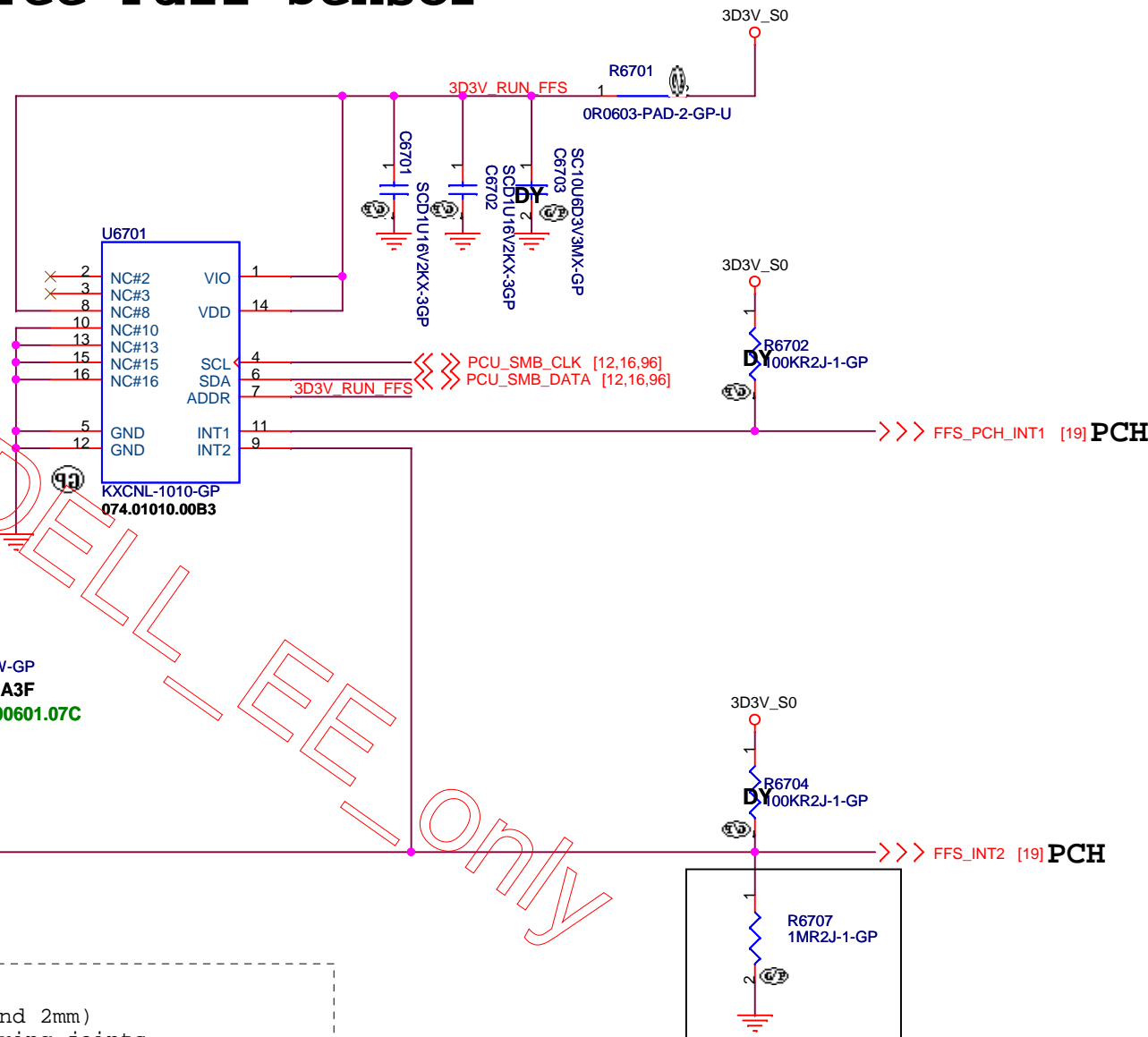
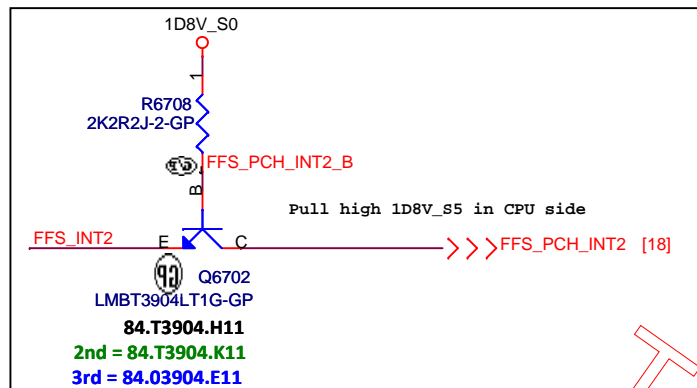
Rev
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Sheet 66 of 109

SSID = User.interface

Free Fall Sensor

For Kionix FFS as SW proposal 5/15



Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

2014.04.24 Venner suggest, reserve to prevent error trigger
2014.08.28 Change R6707 to 63.10534.1DL for common part

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Free Fall Sensor

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Document Number

Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 67 of 109

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Title

Thunderbolt (2/5)

Size
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Plano 11.6" BTM

Rev

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Date: Tuesday, December 16, 2014

Sheet 69 of 109

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Title

Thunderbolt (3/5)

Size
A

Document Number

Plano 11.6" BTM

Rev

A00


Date: Tuesday, December 16, 2014

Sheet 70 of 109

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Title Thunderbolt (4/5)			
Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 71 of	109

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Thunderbolt (5/5)

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Document Number

Plano 11.6" BTM

Rev

A00


Date: Tuesday, December 16, 2014

Sheet 72 of 109

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GPU (1/5) PEG

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Document Number
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 73 of 109

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GPU (2/5) DIGITAL

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Document Number

Plano 11.6" BTM

Rev

A00

Date: Tuesday, December 16, 2014

Sheet 74 of 109

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GPU (3/5) VRAM

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Document Number

Plano 11.6" BTM

Rev

A00

Date: Tuesday, December 16, 2014

Sheet 75 of 109

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Title			
GPU (4/5) GPIO			
Size	Document Number		Rev
A	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014	Sheet 76 of	109

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Title GPU (5/5) PWR/GND			
Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 77 of	109

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Title

VRAM1,2 (1/4)

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Document Number

Plano 11.6" BTM

Rev

A00


Date: Tuesday, December 16, 2014

Sheet 78 of 109

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Size	Document Number		Rev
A	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014	Sheet	79 of 109

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Title

VRAM5,6 (3/4)

Size
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Document Number

Plano 11.6" BTM

Rev

A00


Date: Tuesday, December 16, 2014

Sheet 80 of 109

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A	Plano 11.6" BTM		A00
Date:	Tuesday, December 16, 2014		Sheet 81 of 109

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Title VGA CORE			
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Date: Tuesday, December 16, 2014		Sheet 82 of	109

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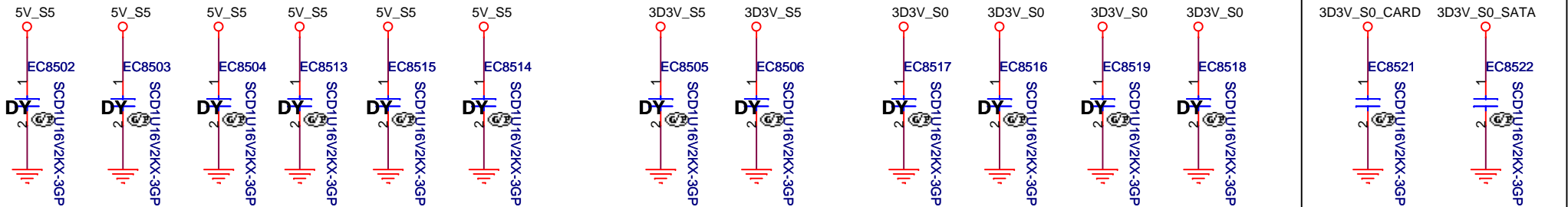
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Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 83 of	109

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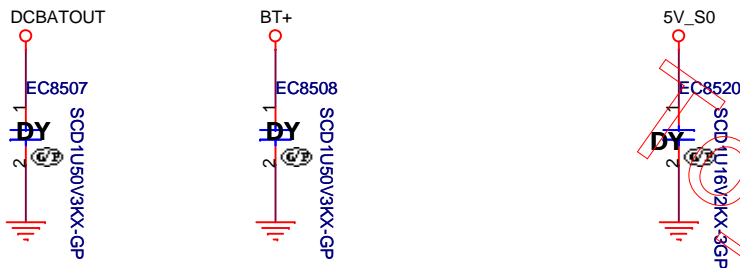
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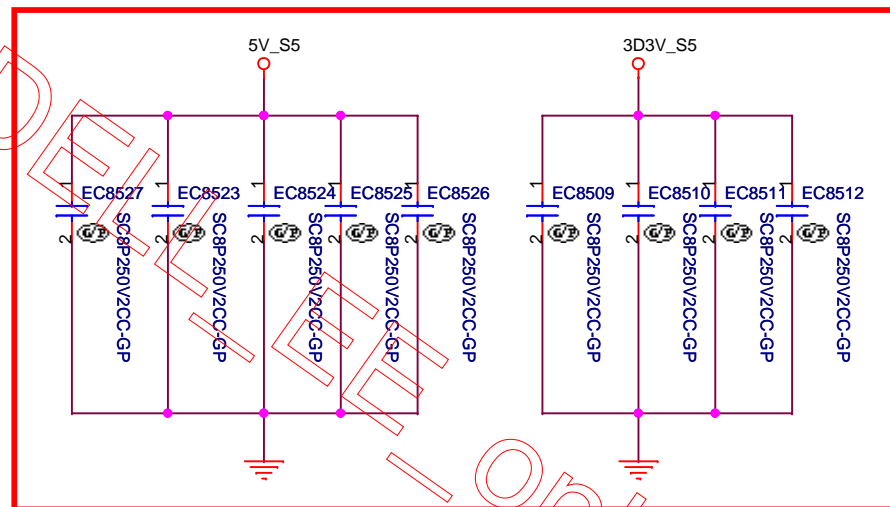
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Title Switchable GFXLCD			
Size A	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 84 of	109



2014.09.03 DVT1 EMC add



10/24/2014 DVT2 add for RF cap

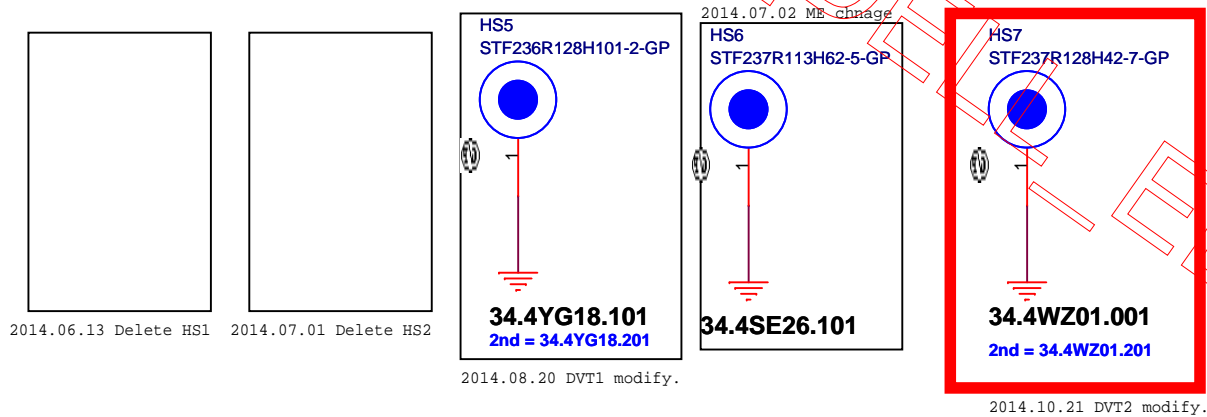
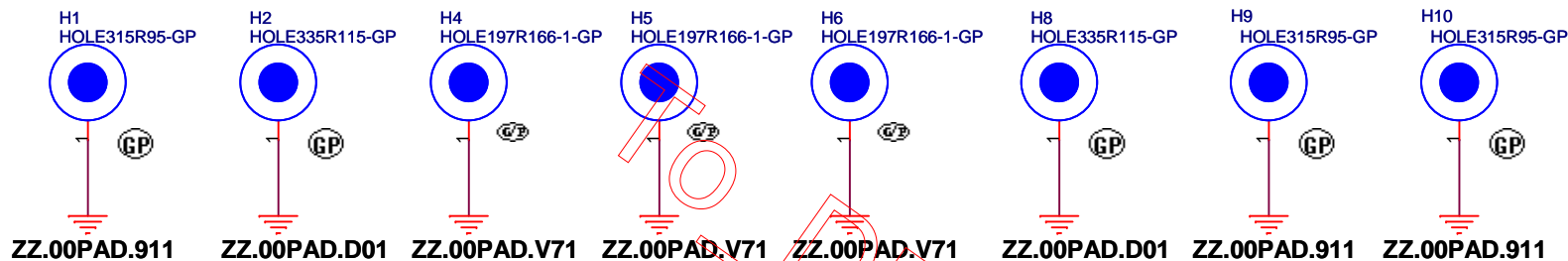
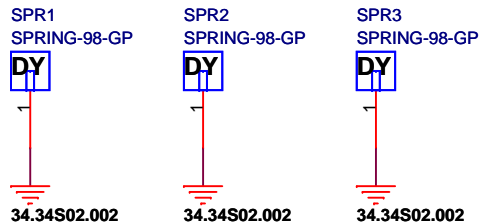


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Title UNUSED PARTS/EMI Capacitors		
Size A4	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014 Sheet 85 of 109		



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UNUSED PARTS/EMI Capacitors					
Size	Document Number				Rev
	Plano 11.6" BTM				A00
Date: Tuesday, December 16, 2014			Sheet	86	of 109

SSID = USH

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Title

USH Board Connector

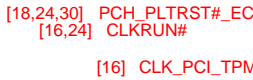
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Document Number
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014Sheet 87 of 109

SSID = TPM



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	<i>Plano 11.6" BTM</i>		<i>A00</i>
Date:	Tuesday, December 16, 2014	Sheet	88 of 109



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Synthesis and Characterization of a New Polymer	Jane Smith	2019	Macromolecules	52	12	789-795
3. Kinetic Study of the Decomposition of Hydrogen Peroxide	Michael Brown	2020	Chemical Kinetics and Catalysis	10	1	123-130
4. The Role of Catalysts in Chemical Reactions	Sarah White	2021	Chemical Reviews	101	5	2345-2360
5. Environmental Impact of Industrial Processes	David Green	2022	Environmental Science and Technology	56	8	5678-5685

TPM

Size

Document Number

Rev

Plano 11.6" BTM

A00


Date: Tuesday, December 16, 2014

Sheet	88	of	109
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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 89	of 109

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Title USB 3.0 Controller			
Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 90 of	109

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Smart Card

Size

Document Number

Rev

Plano 11.6" BTM

A00

Date: Tuesday, December 16, 2014

Sheet 91 of 109

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Size A	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014		Sheet 92 of 109

SSID = Docking

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Size A4	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 93 of	109

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Size A3	Document Number Plano 11.6" BTM		Rev A00
Date: Tuesday, December 16, 2014		Sheet 94 of	109

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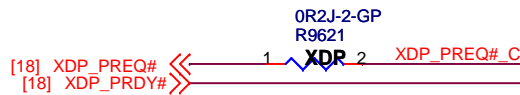
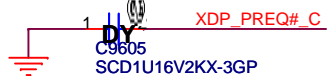
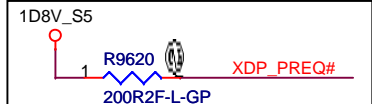
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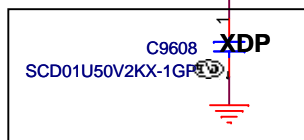
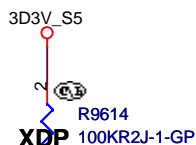
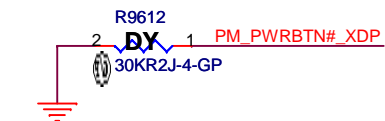
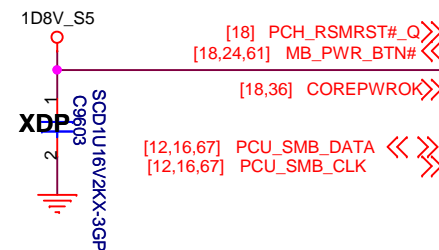
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LAN SW			
Size	Document Number		Rev
A4	Plano 11.6" BTM		A00
Date: Tuesday, December 16, 2014		Sheet 95 of	109

SSID = CPU_XDP

6/19 BTM CRB:200Ω



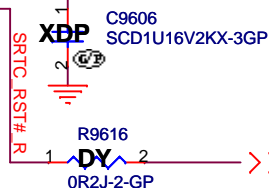
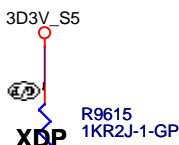
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2014.06.23 Add for sequence

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A00 ZZ.00PAD.Q81

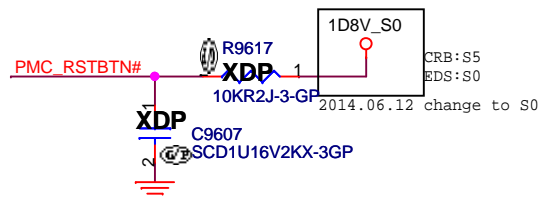
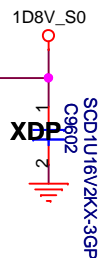
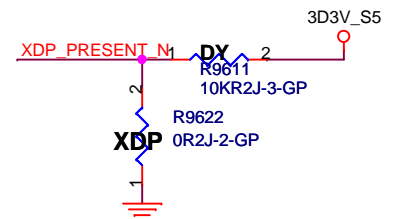
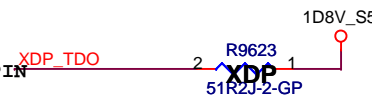


CPU_XDP

(CRB#509728)

Layout Note:

PLACE R9623 WITHIN 0.25" FROM XDP PIN



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Title		
CPU XDP		
Size	Document Number	Rev
A4	Plano 11.6" BTM	A00
Date	Wednesday, December 17, 2014	Sheet 96 of 109

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USB2.0 HUB

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Document Number

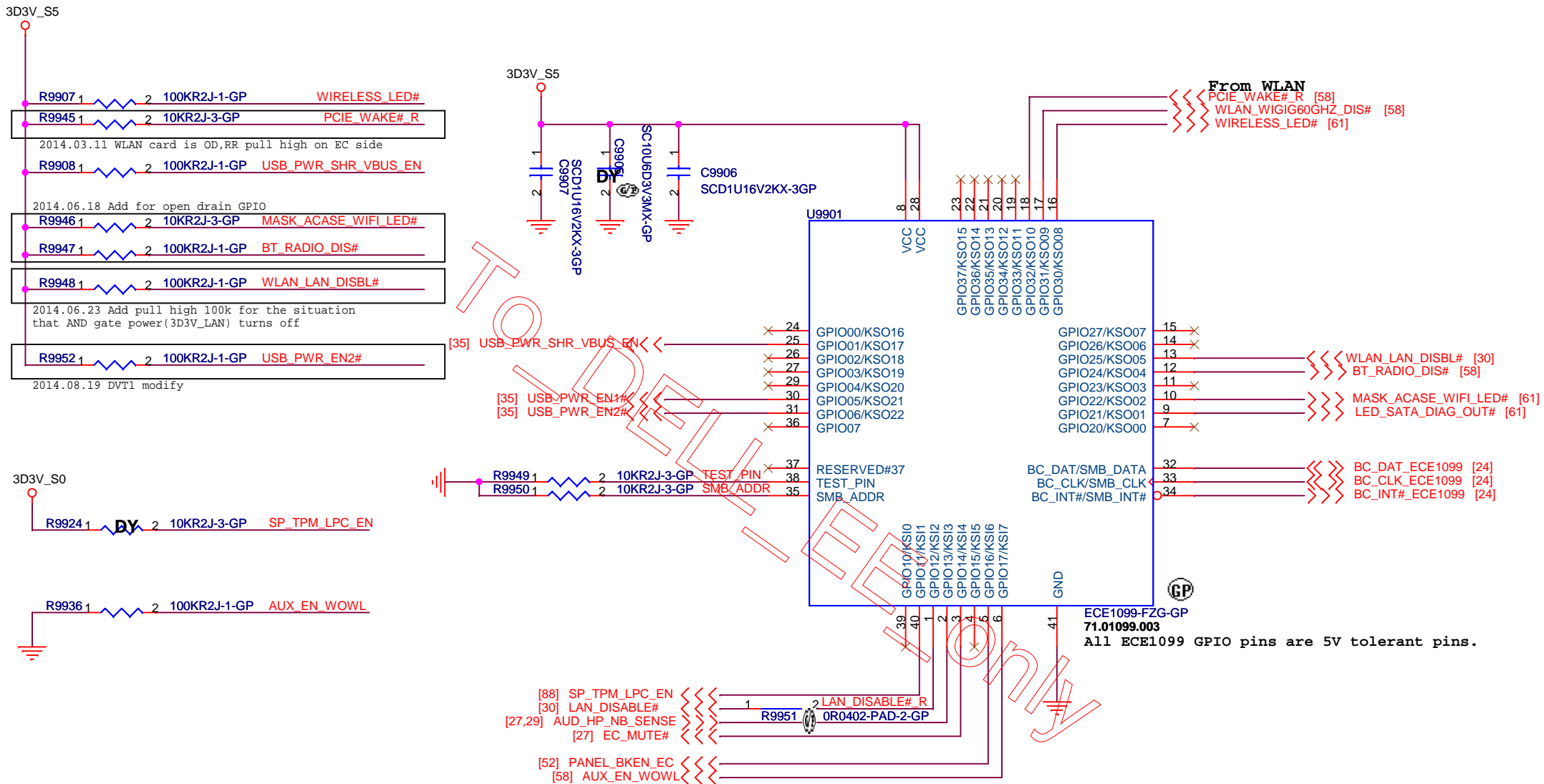
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 97 of 109

SSID = SIO



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Size
A4

Document Number

Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 99 of 109

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2
2	WLAN (BT)
3	CAMERA

USH Side

Pair	Device
0	NA
1	NA

USB HUB Side

Pair	Device
1	NA
2	NA
3	NA
4	NA

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	N/A
3	N/A
4	N/A

PCIE Table

PCIE	
Lane	Device
1	NA
2	Card Reader
3	WLAN
4	LOM

SATA Table

SATA	
Pair	Device
0	HDD
1	NGFF SSD

Processor Strapping

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Bay trail M Processor Schematic Checklist

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Title

Table of Content

Size
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Document Number

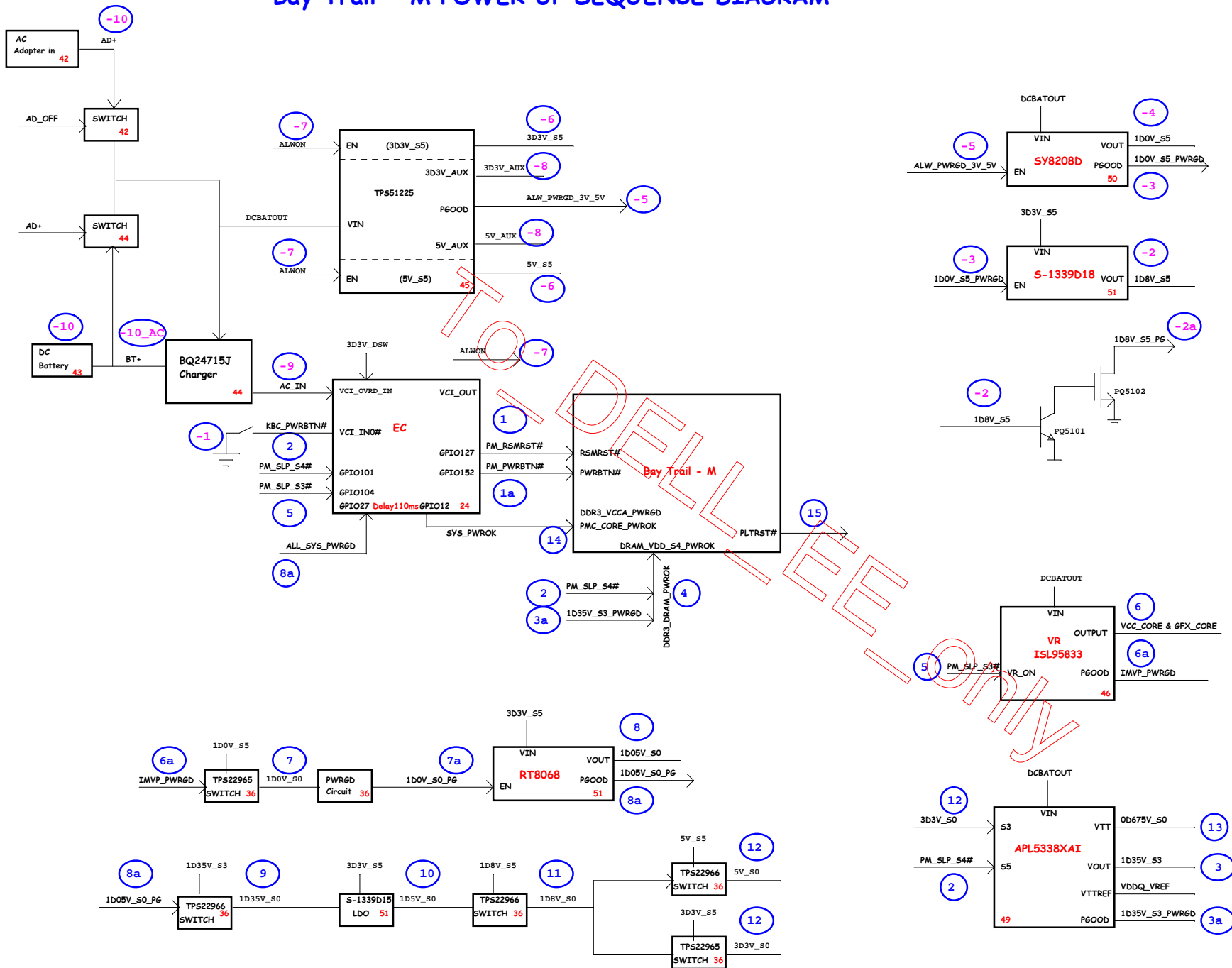
Plano 11.6" BTM

Rev
A00

Date: Tuesday, December 16, 2014

Sheet 100 of 109

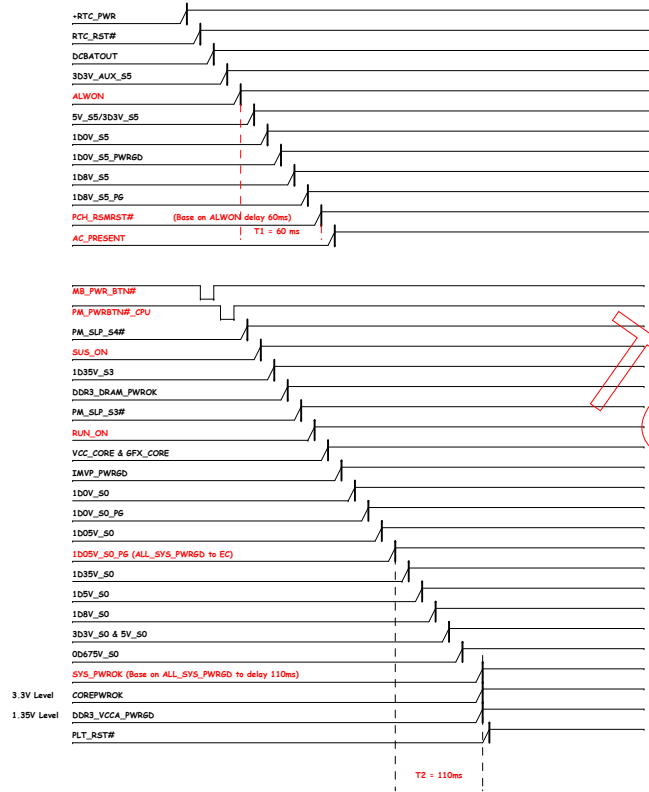
Bay Trail - M POWER UP SEQUENCE DIAGRAM



Intel-Power Up Sequence with non-S0ix

(AC mode)

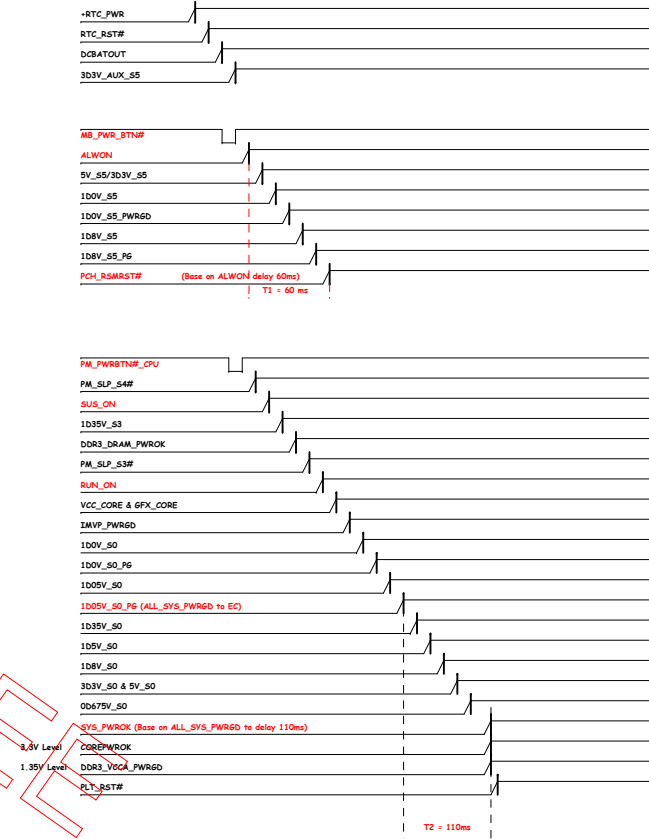
Red word : RBC GPIO



Intel-Power Up Sequence with non-S0ix

(DC mode)

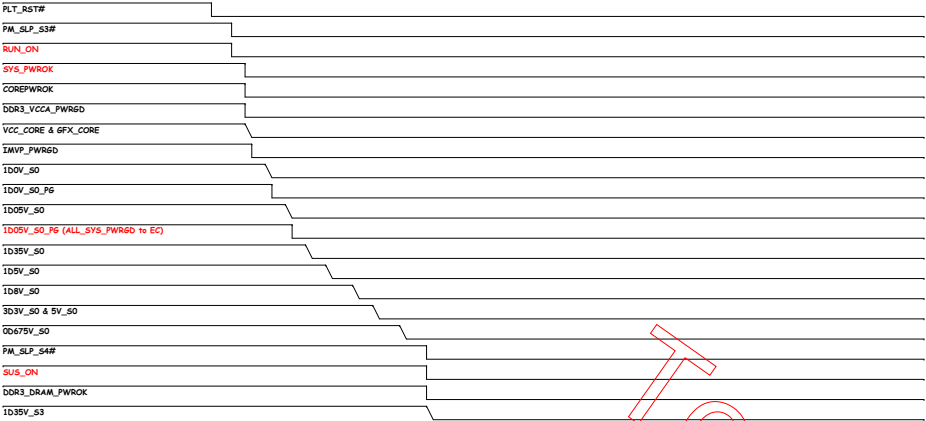
Red word : RBC GPIO



Intel-Power Down Sequence

(AC mode)

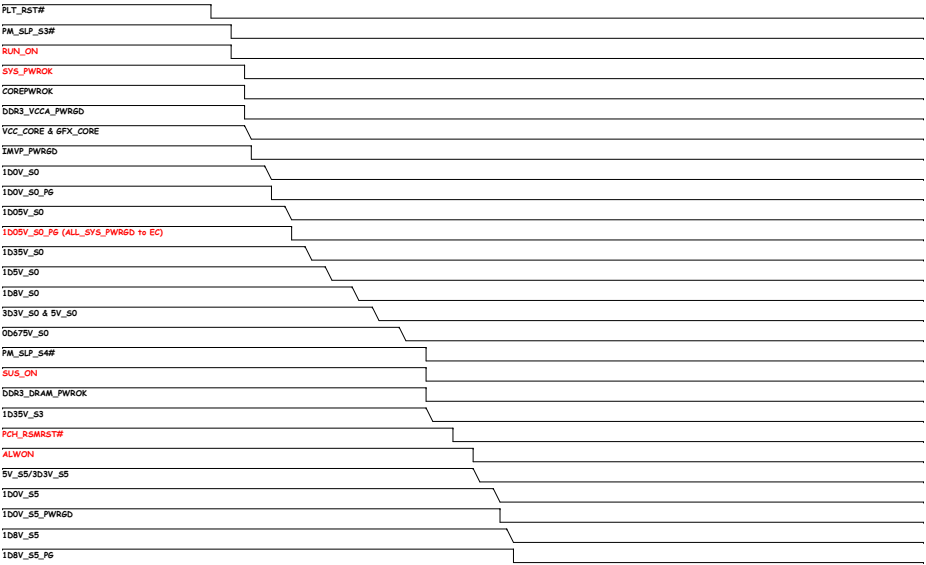
Red word : X8C QP10

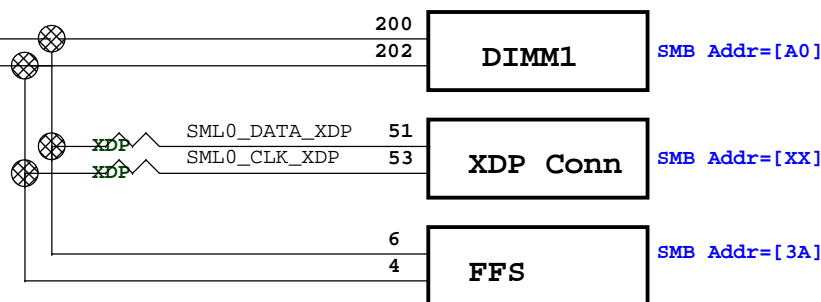
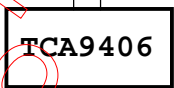
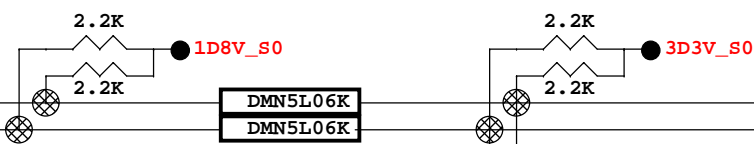
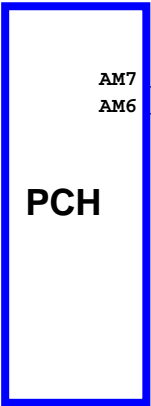


Intel-Power Down Sequence

(DC mode)

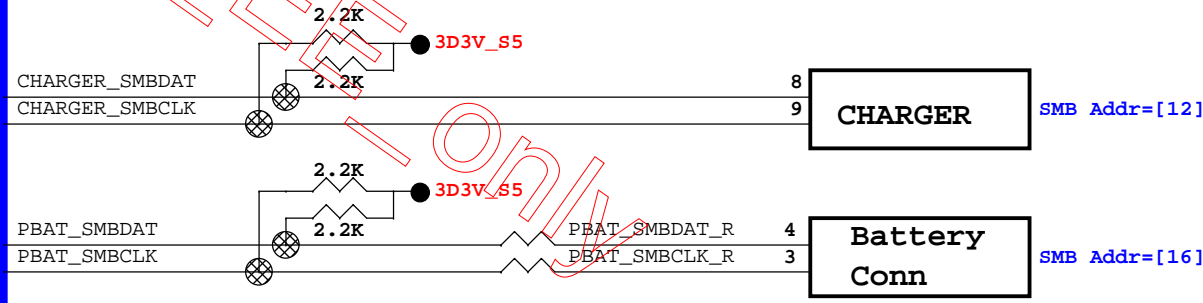
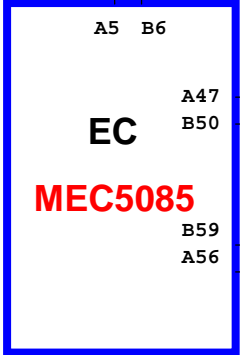
Red word : X8C QP10





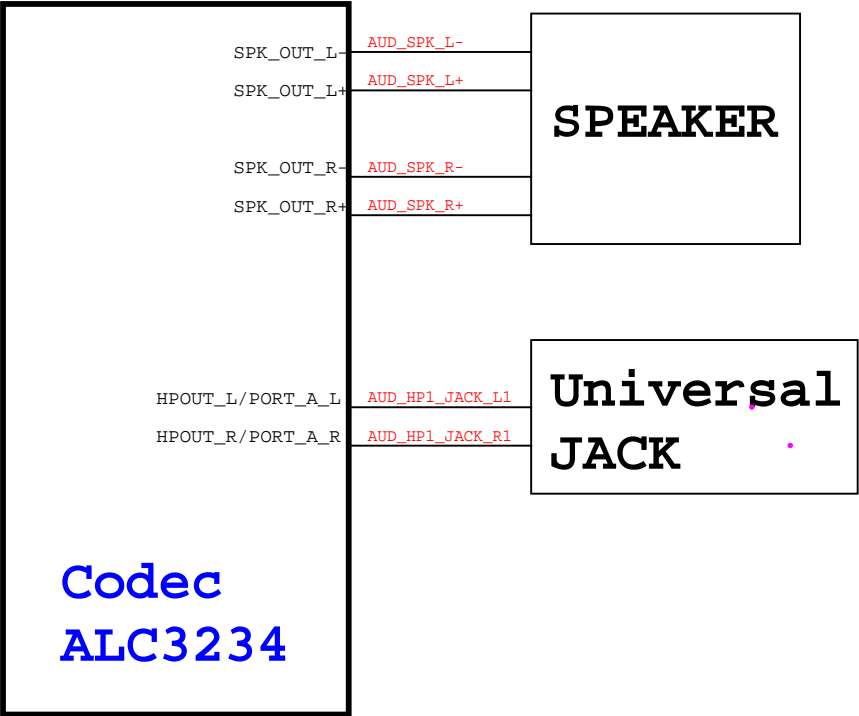
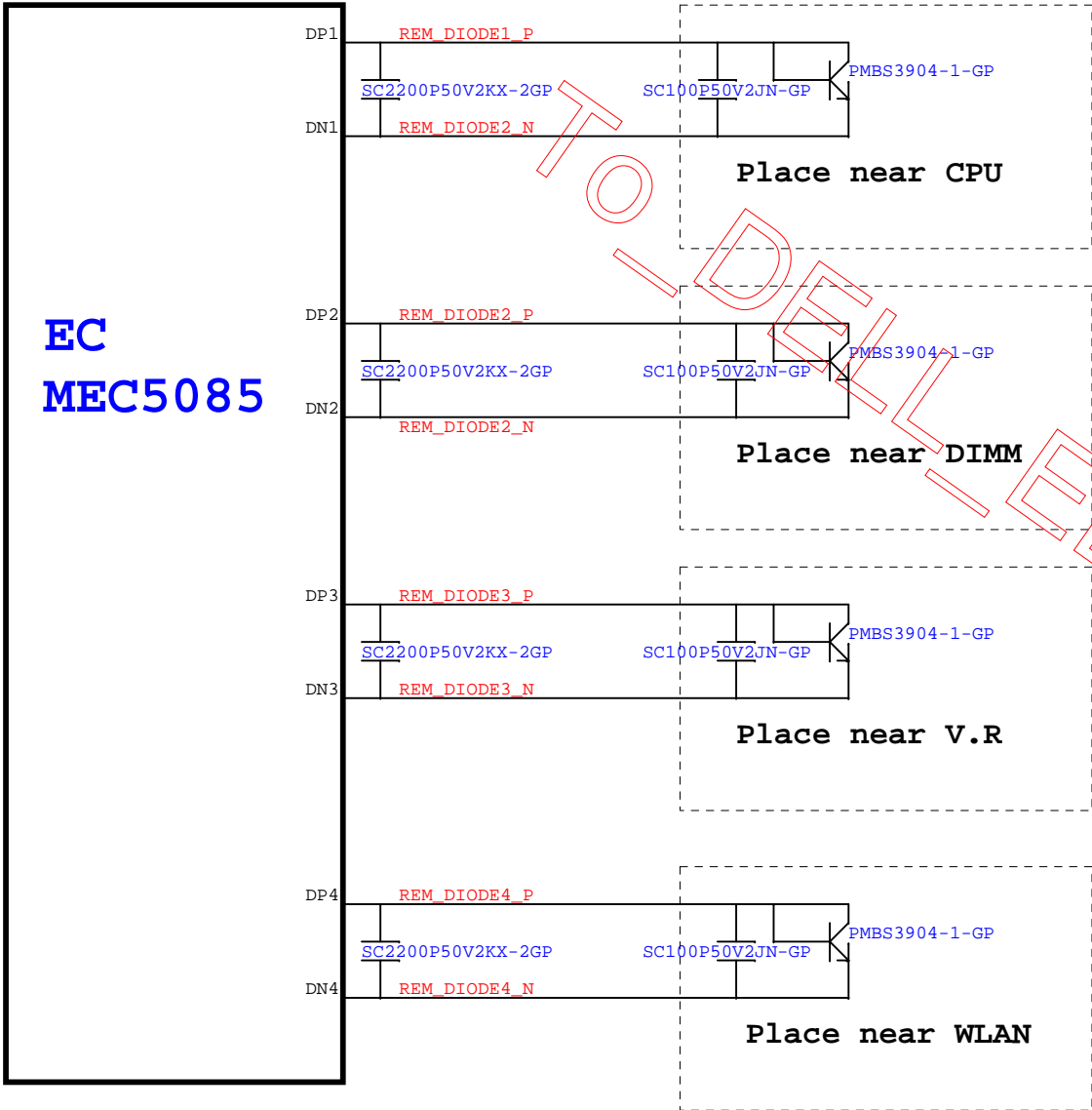
ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

Bus Specification V1.1, which can be downloaded from www.smbus.org. The bq24715/7 uses the SMBus Read-Word and Write-Word protocols (Figure 4) to communicate with the smart battery. The bq24715/7 performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In



Thermal Block Diagram

Audio Block Diagram



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<i>Thermal/Audio Block Diagram</i>			
Size	Document Number		Rev
	<i>Plano 11.6" BTM</i>		<i>A00</i>
Date:	Tuesday, December 16, 2014	Sheet 105 of	109

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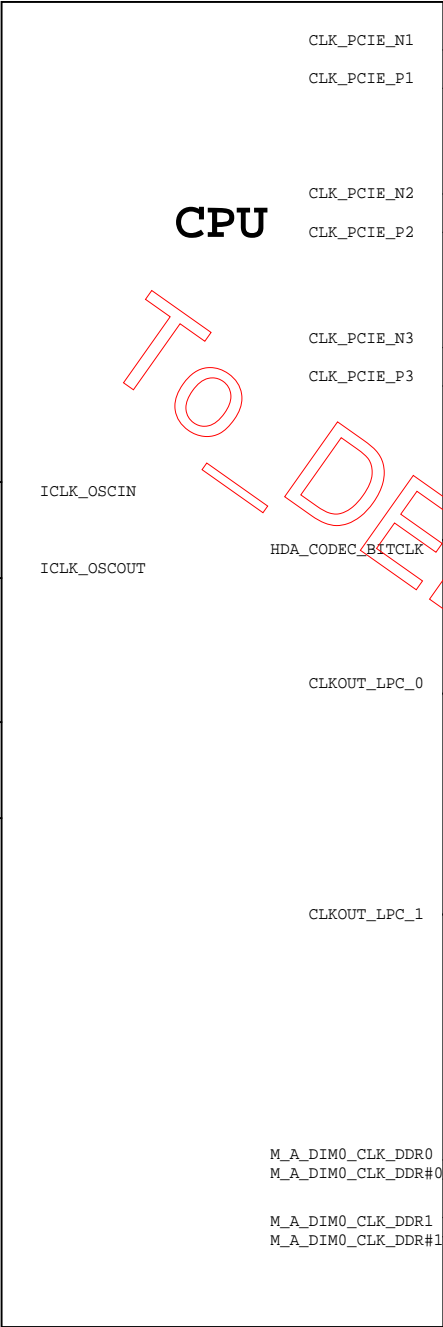
C

B

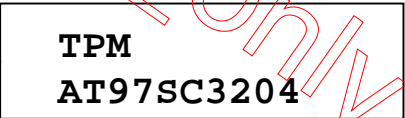
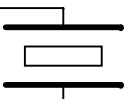
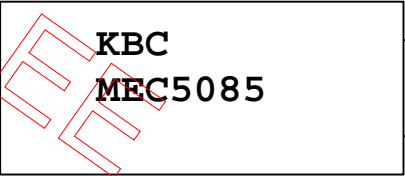
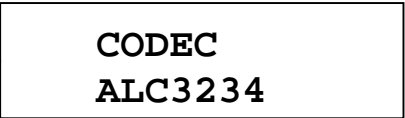
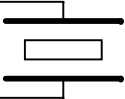
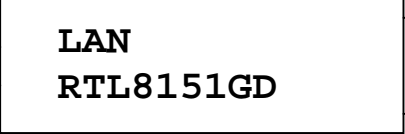
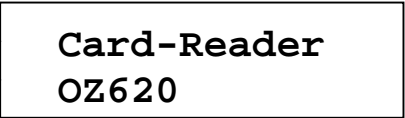
A

X1801
25MHZ

X1802
32.768kHz



CPU



<Core Design>

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Title		
CLK Block		
Size A4	Document Number Plano 11.6" BTM	Rev A00
Date: Tuesday, December 16, 2014	Sheet 106 of	109